8 Small Signal Analysis of Amplifiers

Learning Objectives

After completing this chapter you, will learn the following:

- Frequency response of amplifiers.
- h-parameter model of amplifiers.
- h-parameter model of BJT amplifiers.
- Analysis of different BJT amplifier configurations using h-parameters.
- Small signal response of FET amplifiers.
- Cascading amplifiers.
- Darlington amplifiers.
- Cascode amplifiers.
- Low-frequency response of BJT amplifiers.
- Low-frequency response of FET amplifiers.
- Effect of cascading amplifier stages on the overall frequency response.

The chapter focuses on the small signal response of BJT and FET amplifiers. The small signal response of BJT amplifiers is mostly analyzed using the h-parameter model. In the chapter, the h-parameter model for the three BJT configurations is covered and detailed analysis of BJT amplifiers using the h-parameter model has been carried out. The small signal response of FET amplifiers is also discussed. In addition to the mid-band analysis, the low-frequency response of both BJT and FET amplifiers is also discussed in the chapter.

Cascading of amplifiers is done to increase the value of gain, to match the input and output impedances of the amplifier with the source and the load impedance, respectively. Cascading of BJT and FET amplifiers with particular reference to its effect on the overall frequency response of the amplifier is also described. Other topics covered in the chapter include Darlington amplifiers and Cascode amplifiers.

8.1 Amplifier Bandwidth: General Frequency Considerations

The response of an amplifier to an input signal depends upon the frequency of the signal. Figure 8.1 shows the typical frequency response curves for the RC-coupled, transformer-coupled and the direct-coupled amplifiers. The horizontal scale is a logarithmic scale to permit the plot to highlight both the low-frequency and the high-frequency regions of the response curve. For each curve three regions have been defined, namely, the low-frequency region, the mid-frequency region and the high-frequency region.

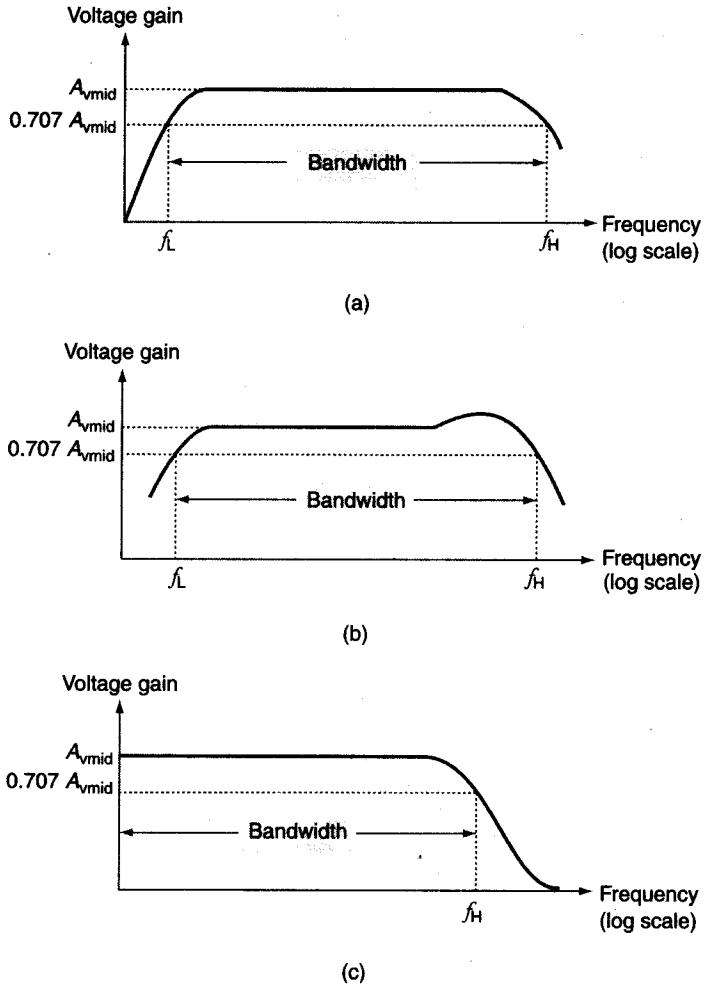


Figure 8.1 (a) Typical frequency response curve of RC-coupled amplifier; (b) typical frequency response curve of transformer-coupled amplifier; (c) typical frequency response curve of direct-coupled amplifier.

Low-frequency response of an amplifier is affected by the input and the output coupling capacitors and the bypass capacitors. At low frequencies, these capacitors cannot be replaced by short-circuit approximations as their reactances increase at low frequencies. The stray capacitances and the capacitive elements related to the active device and the network limit the high-frequency response of the system.

For each amplifier there is a region of frequencies where the magnitude of gain is relatively close to the mid-band value. The cut-off levels are defined by the frequencies where the gain value in decibels falls below the mid-band value by 3 decibels. In other words, the cut-off frequencies are defined as those frequencies where the magnitude of the gain in 0.707 times its value at the mid-band frequencies or the magnitude of the power gain is half of the magnitude of the power gain at the mid-band frequencies. The cut-off frequencies are referred to as the lower cut-off frequency (f_L) and the upper cut-off frequency (f_H). The difference between the upper cut-off and the lower cut-off frequencies is referred to as the bandwidth of the system.

8.2 Hybrid h-Parameter Model for an Amplifier

A two-port, four-terminal device or an amplifier (Figure 8.2) with two input and two output terminals can be represented in terms of an equivalent circuit model making use of two currents and two voltages provided that it meets the following two conditions. First, there is a common connection between the input and the output. Second, it should contain only linear elements. Two of the four variables (input and output currents, input and output voltages) can be chosen as the independent variables and the remaining two variables can be expressed in terms of these independent variables. The choice of the independent variables depends upon the nature of the device.

Transistors are generally modeled using the hybrid parameter model or the h-parameter model and the transistor datasheets provide the values of the h-parameters. Hence, the hybrid parameter model is described here in detail. In the case of h-parameter model, input current (I_i) and output voltage (V_o) are taken as independent variables. The other two variables, namely, the input voltage (V_i) and the output current (I_o) are related to these variables by the following equations:

$$V_i = h_{11}I_i + h_{12}V_o \tag{8.1}$$

$$I_o = h_{21}I_i + h_{22}V_o \tag{8.2}$$

The quantities h_{11}, h_{12}, h_{21} and h_{22} are referred to as the hybrid parameters or the h-parameters. The term "hybrid" is chosen as these terms have different dimensions, that is, they are not alike dimensionally. Figure 8.3 shows the representation of the network in terms of the h-parameters. As we can see from the figure, the h-parameter model makes use of the Thevenin's voltage equivalent model at the input and the Norton's current equivalent model at the output. It may be mentioned here that V_i and I_i are the RMS voltage and current values, respectively, of the applied input signal. V_o and I_o are the RMS voltage and current values of the resulting output signal.

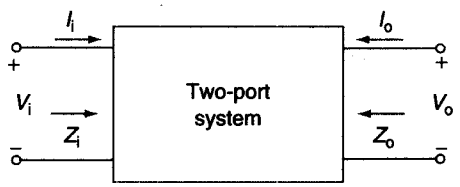


Figure 8.2 | Block diagram of a two-port, four-terminal device.

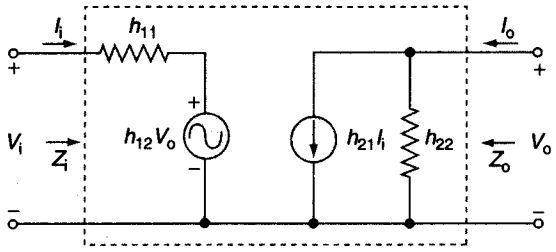


Figure 8.3 | h-parameter model of a two-port network.

Determination of h-Parameters

1. **Parameter h_{11}:** In Eq. (8.1), substituting $V_o = 0$, that is, the output terminals are short circuited, we get

$$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o = 0} \tag{8.3}$$

where V_i and I_i are the RMS values of input voltage and current, respectively. Using partial calculus, the value of h_{11} can be calculated as

$$h_{11} = \left.\frac{\partial v_i}{\partial i_i}\right|_{V_o = \text{const.}} = \left.\frac{\Delta v_i}{\Delta i_i}\right|_{V_o = \text{const.}} \tag{8.4}$$

Therefore, the parameter h_{11} is the ratio of the instantaneous change in the input voltage to the instantaneous change in the input current for constant value of output voltage. Hence, the parameter h_{11} has the units of impendance, that is, ohms. It is referred to as the short-circuit input impedance parameter. The subscript 11 indicates that it is dependent on the values of the input quantities. h_{11} is also represented as h_i.

2. **Parameter h_{12}:** In Eq. (8.1), if we substitute $I_i = 0$, that is, the input terminals are open circuited, then

$$h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i = 0} \tag{8.5}$$

Using partial calculus, the value of h_{12} can be determined as

$$h_{12} = \left.\frac{\partial v_i}{\partial v_o}\right|_{I_i = \text{const.}} = \left.\frac{\Delta v_i}{\Delta v_o}\right|_{I_i = \text{const.}} \tag{8.6}$$

Here h_{12} is the ratio of the instantaneous change in the input voltage to the instantaneous change in the output voltage for constant value of input current and is referred to as the open-circuit reverse transfer voltage ratio parameter. It is a dimensionless quantity. h_{12} is also represented as h_r.

3. **Parameter h_{21}:** If in Eq. (8.2), we substitute $V_o = 0$, that is, the output terminals are shorted, then

$$h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o = 0} \tag{8.7}$$

Applying partial calculus, the value of h_{21} is given by

$$h_{21} = \left.\frac{\partial i_o}{\partial i_i}\right|_{V_o = \text{const.}} = \left.\frac{\Delta i_o}{\Delta i_i}\right|_{V_o = \text{const.}} \tag{8.8}$$

Parameter h_{21} is the ratio of the change in the instantaneous value of output current to the change in the instantaneous value of the input current for constant value of output voltage. It is dimensionless parameter and is referred to as the short-circuit forward transfer current ratio parameter. h_{21} is also represented as h_f.

4. **Parameter h_{22}:** If the input terminals are open circuit, that is, $I_i = 0$, then Eq. (8.2) simplifies to

$$h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i = 0} \tag{8.9}$$

Applying partial calculus we get

$$h_{22} = \left.\frac{\partial i_o}{\partial v_o}\right|_{I_i = \text{const.}} = \left.\frac{\Delta i_o}{\Delta v_o}\right|_{I_i = \text{const.}} \tag{8.10}$$

Parameter h_{22} is the ratio of the change in the instantaneous value of output current to the change in the instantaneous value of the output voltage for constant value of input current. It is referred to as the open-circuit output admittance parameter and is measured in siemens. h_{22} is also represented as h_o.

8.3 Transistor Hybrid Model

The h-parameter model is widely used for bipolar junction transistors. The basic assumption here is that the variations in the Q-point are small, so that the transistor parameters can be considered constant over the complete signal excursion. It may be mentioned here that the h-parameter model is applicable to all the three transistor configurations. The values of h-parameters are more or less constant for a given transistor, although they vary slightly with change in collector current. However, they have different values for each of the three transistor configurations. In this section we discuss the h-parameter model for the three transistor configurations.

h-Parameter Model for the Common-Emitter Configuration

Figures 8.4(a) and (b) show the circuit symbol and the h-parameter equivalent model for the common-emitter configuration, respectively. As we can see from the figure, a second subscript has been added to the nomenclature of the h-parameters. This is done so as to distinguish between the h-parameters of the three transistor configurations. The parameter h_{11} is denoted as h_{ie} and is referred to as the input impedance of the transistor in the common-emitter configuration. Parameter h_{21} is denoted as h_{fe} and stands for forward current transfer ratio for the common-emitter transistor configuration; parameter h_{12} is denoted as h_{re} and is referred to as the reverse voltage transfer ratio for the common-emitter transistor configuration. Parameter h_{22} is denoted as h_{oe} and it means the output admittance for the common-emitter configuration. Note that in this case, current I_i is the base current I_b, current I_o is the collector current I_c, voltage V_i is the voltage V_{be} and voltage V_o is the voltage V_{ce}. The h-parameter equations for the common-emitter configuration are given by the following two equations:

$$V_{be} = h_{ie} I_b + h_{re} V_{ce} \tag{8.11}$$

$$I_c = h_{fe} I_b + h_{oe} V_{ce} \tag{8.12}$$

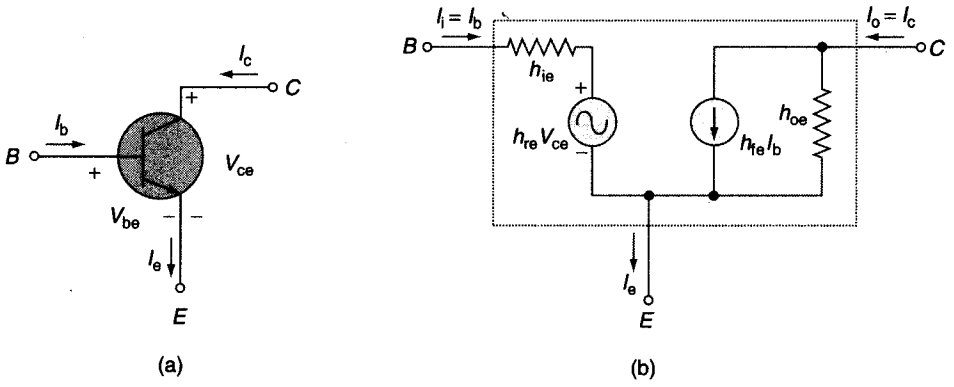


Figure 8.4 (a) Circuit symbol of common-emitter transistor configuration; (b) h-parameter model for the common-emitter transistor configuration.

The values of the parameters h_{ie}, h_{fe}, h_{re} and h_{oe} are given by the following set of equations, respectively.

$$h_{ie} = \left.\frac{\partial v_{be}}{\partial i_b}\right|_{V_{ce} = \text{const.}} = \left.\frac{\Delta v_{be}}{\Delta i_b}\right|_{V_{ce} = \text{const.}} \tag{8.13}$$

$$h_{re} = \left.\frac{\partial v_{be}}{\partial v_{ce}}\right|_{I_b = \text{const.}} = \left.\frac{\Delta v_{be}}{\Delta v_{ce}}\right|_{I_b = \text{const.}} \tag{8.14}$$

$$h_{fe} = \left.\frac{\partial i_c}{\partial i_b}\right|_{V_{ce} = \text{const.}} = \left.\frac{\Delta i_c}{\Delta i_b}\right|_{V_{ce} = \text{const.}} \tag{8.15}$$

$$h_{oe} = \left.\frac{\partial i_c}{\partial v_{ce}}\right|_{I_b = \text{const.}} = \left.\frac{\Delta i_c}{\Delta v_{ce}}\right|_{I_b = \text{const.}} \tag{8.16}$$

The symbol Δ refers to a small variation around the quiescent point of operation, that is, the h-parameters are determined in the region of operation for the applied signal. The effect of the parameter h_{re} is so small on the transistor amplifier that it can be neglected. Figure 8.5 shows the simplified h-parameter model for the common-emitter transistor configuration. Here, h_{re} is assumed to be zero, therefore the magnitude of the voltage source $h_{re}V_{ce}$ is also equal to zero. In other words, it results in short-circuit equivalent for the feedback element. In cases where the value of $1/h_{oe}$ is very large as compared to the value of load resistance, it is assumed to be open in comparison with the parallel load to be connected across the output terminals.

Figures 8.6(a), (b) and (c) respectively show the circuit symbol, complete h-parameter model and simplified h-parameter model of the common-collector configuration. The parameter h_{ic} is referred to as the input impedance of the transistor in the common-collector configuration. Parameter h_{fc} stands for forward current transfer ratio for the common-collector configuration and parameter h_{rc} is referred to as the reverse voltage transfer ratio for the common-collector configuration. Parameter h_{oc} is the output admittance in the common-collector configuration. The h-parameters for the common-collector configuration can be determined in a similar fashion as that for the common-emitter configuration.

Figures 8.7(a), (b) and (c) respectively show the circuit symbol, complete h-parameter model and the simplified h-parameter model for the common-base configuration. h_{ib} is the input impedance parameter, h_{fb} is the forward current transfer ratio, h_{rb} is the reverse voltage transfer ratio and h_{ob} is the output admittance parameter for the common-base configuration.

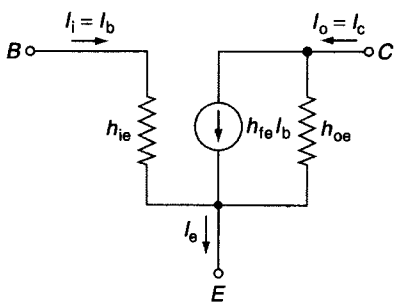


Figure 8.5 | Simplified h-parameter model for the common-emitter transistor configuration.

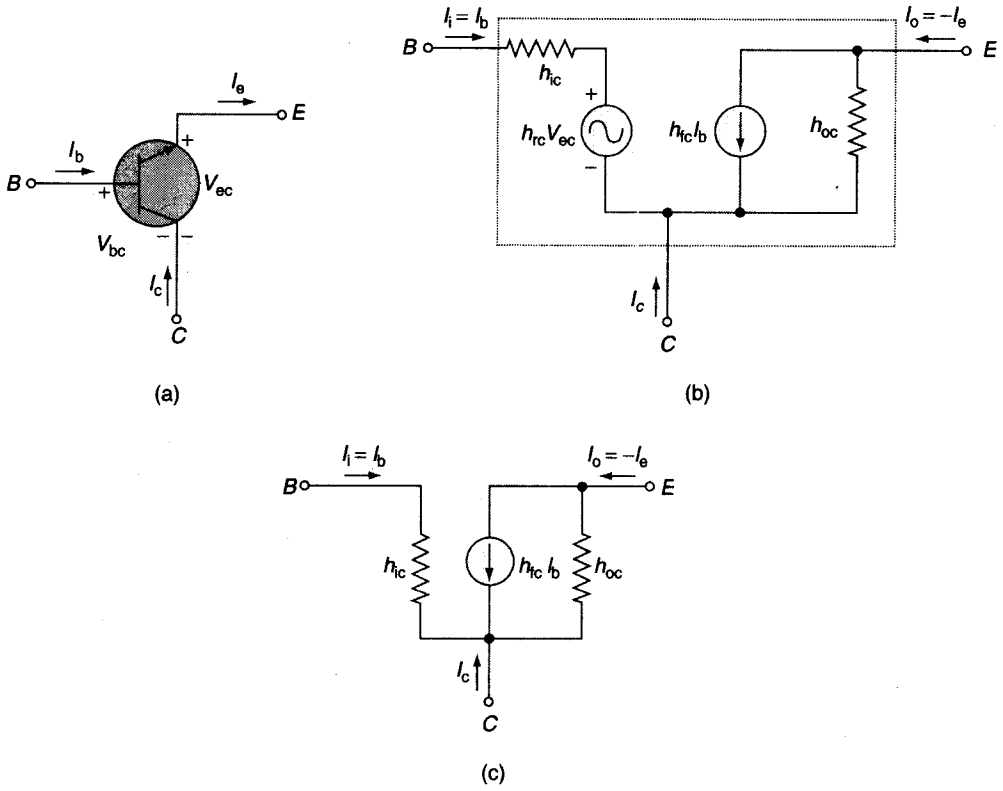


Figure 8.6 | Common-collector transistor configuration: (a) Circuit symbol; (b) h-parameter model; (c) simplified h-parameter model.

Relationships between h-Parameters of Different Transistor Configurations

While designing a transistor-based amplifier, it may be necessary to convert from one set of transistor's h-parameters of a given configuration to another for the other configurations. Table 8.1 gives the approximate conversion formulae for the h-parameters. Derivation of the formulae is beyond the scope of the book.

Table 8.1 | Approximate conversion formulae for the h-parameters

$h_{ic} = h_{ie}$	$h_{rc} = 1$	$h_{fc} = -(1 + h_{fe})$	$h_{oc} = h_{oe}$
$h_{ib} = \dfrac{h_{ie}}{1 + h_{fe}}$	$h_{rb} = \dfrac{h_{ie}h_{oe}}{1 + h_{fe}} - h_{re}$	$h_{fb} = -\dfrac{h_{fe}}{1 + h_{fe}}$	$h_{ob} = \dfrac{h_{oe}}{1 + h_{fe}}$
$h_{ie} = \dfrac{h_{ib}}{1 + h_{fb}}$	$h_{re} = \dfrac{h_{ib}h_{ob}}{1 + h_{fb}} - h_{rb}$	$h_{fe} = -\dfrac{h_{fb}}{1 + h_{fb}}$	$h_{oe} = \dfrac{h_{ob}}{1 + h_{fb}}$
$h_{ic} = \dfrac{h_{ib}}{1 + h_{fb}}$	$h_{rc} = 1$	$h_{fc} = -\dfrac{1}{1 + h_{fb}}$	$h_{oc} = \dfrac{h_{ob}}{1 + h_{fb}}$

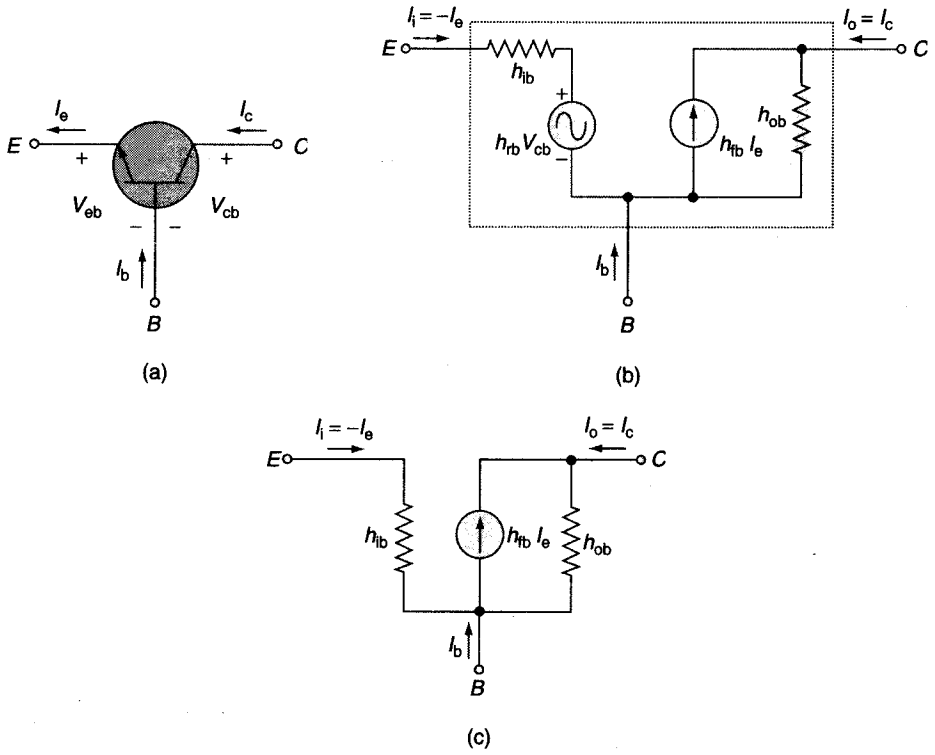


Figure 8.7 Common-base transistor configuration: (a) Circuit symbol; (b) h-parameter model; (c) simplified h-parameter model.

EXAMPLE 8.1

Given that the hybrid parameters for the transistor are h_{ie} = 1.5 kΩ, h_{fe} = 150, $h_{re} = 1 \times 10^{-4}$ and h_{oe} = 20 μmhos. Draw the hybrid equivalent circuit of the transistor in all the three configurations.

Solution

1. Figure 8.8(a) shows the hybrid equivalent circuit for the transistor in the common-emitter configuration.
2. The values of hybrid parameters in the common-collector configuration are
$$h_{ic} = h_{ie},\ h_{rc} = 1,\ h_{fc} = -(1 + h_{fe}) \text{ and } h_{oc} = h_{oe}$$
3. Therefore, h_{ic} = 1.5 kΩ, h_{rc} = 1, h_{fc} = −151 and h_{oc} = 20 μmhos.
4. Figure 8.8(b) shows the hybrid equivalent circuit of the transistor in the common-collector configuration.
5. The values of hybrid parameters in the common-base configuration are
$$h_{ib} = \frac{h_{ie}}{1 + h_{fe}}$$
$$= (1.5 \times 10^3)/151 = 9.93\ \Omega$$

$$h_{rb} = \frac{h_{ie}h_{oe}}{1+h_{fe}} - h_{re}$$
$$= [(1.5\times10^{3}\times20\times10^{-6})/151] - 1\times10^{-4} = 0.99\times10^{-4}$$

$$h_{fb} = -\frac{h_{fe}}{1+h_{fe}}$$
$$= -150/151 = -0.99$$

$$h_{ob} = \frac{h_{oe}}{1+h_{fe}}$$
$$= (20\times10^{-6})/151 = 0.13\times10^{-6}$$

6. Figure 8.8(c) shows the hybrid equivalent of the transistor in the common-base configuration.

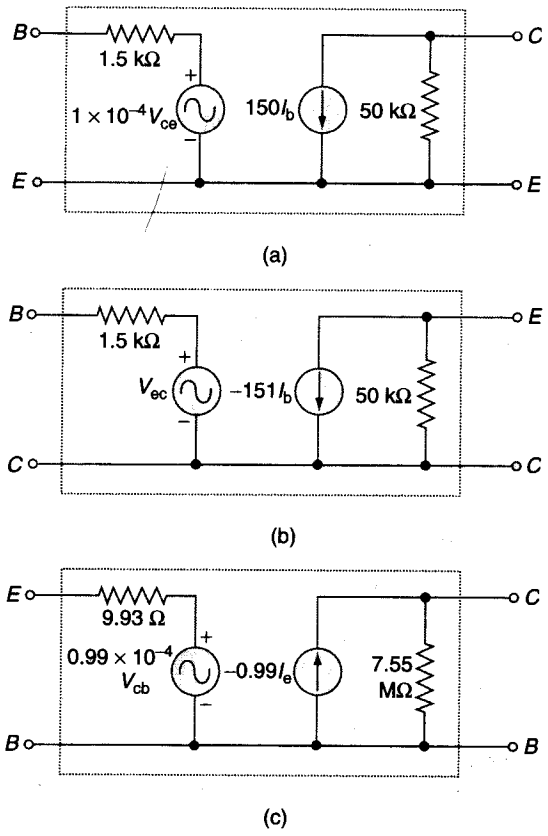


Figure 8.8 | Solution to Example 8.1.

Graphical Determination of h-Parameters

The values of the h-parameters can be determined graphically by making use of the transistor's input and output characteristics. The parameters h_i and h_r are determined from the input characteristic curves of the transistor whereas the parameters h_f and h_o are determined from the output characteristic curves. In this section we describe the procedure for determining the h-parameters graphically for common-emitter transistor configuration. The procedure for determining the h-parameters of the common-base and common-collector configurations is similar to that for the common-emitter configuration.

The first step in determining the h-parameters is to determine the Q-point or the operating point. Figure 8.9 shows the typical input characteristic curve for a transistor in the common-emitter configuration. As we can see from the characteristic curve, the values of the emitter–base voltage, collector–emitter voltage and the base current at the Q-point are given by V_{BEQ}, V_{CEQ} and I_{BQ}, respectively. The parameter h_{ie} is determined by drawing a line tangent to the input characteristic curve corresponding to V_{CEQ} at the Q-point. The value of the parameter h_{ie} is given by the slope of this line. In other words, h_{ie} is the ratio of small change in the value of emitter–base voltage to the small change in the value of base current around the operating point as shown in the figure. Therefore, the value of h_{ie} is given by

$$h_{ie} = \left.\frac{V_{BE2} - V_{BE1}}{I_{B2} - I_{B1}}\right|_{V_{CE} = V_{CEQ}} = \left.\frac{\Delta v_{be}}{\Delta i_b}\right|_{V_{CE} = V_{CEQ}} \tag{8.17}$$

The parameter h_{re} is also determined using the input characteristic curve (Figure 8.10). A horizontal line is drawn at I_B equal to I_{BQ}, that is, for the value of the base current equal to the quiescent value of the base current. The change in emitter–base voltage is determined for a small change in the value of collector–emitter voltage around the operating point. The value of h_{re} is then determined by the ratio of the change in the value of emitter–base

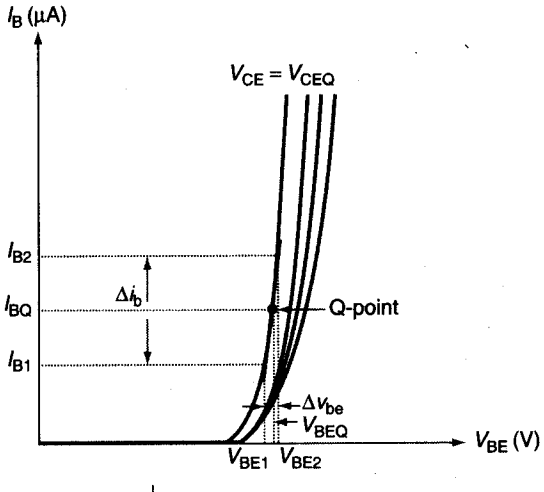


Figure 8.9 | Determination of h-parameter h_{ie}.

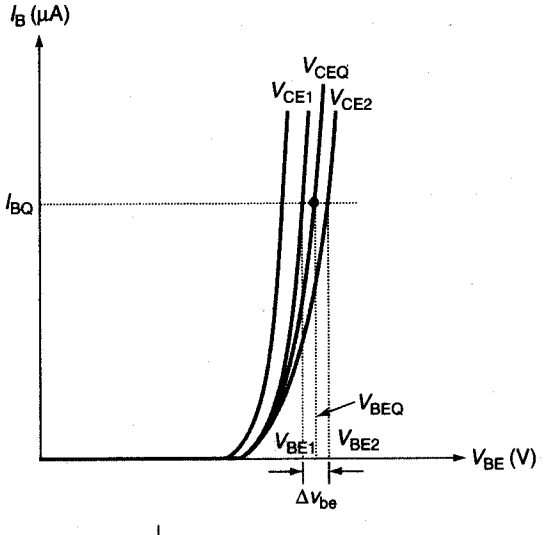


Figure 8.10 | Determination of h-parameter h_{re}.

voltage to the change in the value of collector–emitter voltage for a constant value of base current. The value of h_{re} is given by

$$h_{re} = \left.\frac{V_{BE2} - V_{BE1}}{V_{CE2} - V_{CE1}}\right|_{I_B = I_{BQ}} = \left.\frac{\Delta v_{be}}{\Delta v_{ce}}\right|_{I_B = I_{BQ}} \tag{8.18}$$

The other two parameters, that is, h_{fe} and h_{oe} are determined from the output characteristics. The value of parameter h_{fe} is determined by drawing a vertical line corresponding to the quiescent value of collector–emitter voltage (V_{CEQ}). The value of h_{fe} is then determined by taking a small change in the base current and then determining the corresponding change in the collector current. h_{fe} is the ratio of the change in the collector current to the change in the base current (Figure 8.11). It may be mentioned here that the accuracy of the results improves for small values of the changes. The value of h_{fe} is given by

$$h_{fe} = \left.\frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}}\right|_{V_{CE} = V_{CEQ}} = \left.\frac{\Delta i_c}{\Delta i_b}\right|_{V_{CE} = V_{CEQ}} \tag{8.19}$$

The value of the parameter h_{oe} is determined by drawing a tangent to the output curve corresponding to base current equal to the quiescent base current. The value of the h_{oe} parameter is then determined by taking the ratio of the change in the collector current corresponding to a small change in the collector–emitter voltage (Figure 8.12). The value of h_{oe} is given by

$$h_{oe} = \left.\frac{I_{C2} - I_{C1}}{V_{CE2} - V_{CE1}}\right|_{I_B = I_{BQ}} = \left.\frac{\Delta i_c}{\Delta v_{ce}}\right|_{I_B = I_{BQ}} \tag{8.20}$$

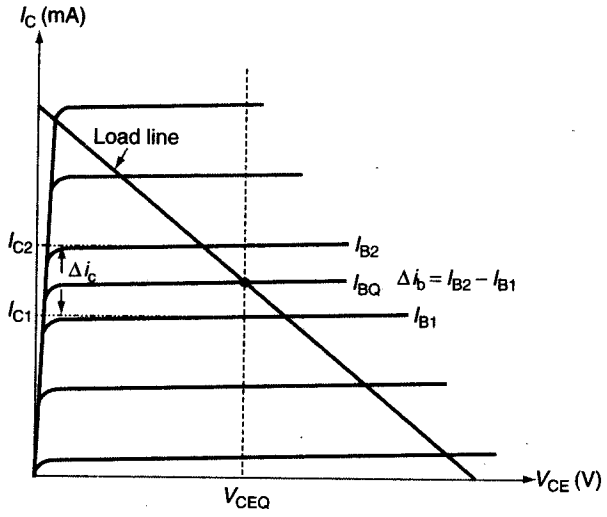


Figure 8.11 | Determination of h-parameter h_{fe}.

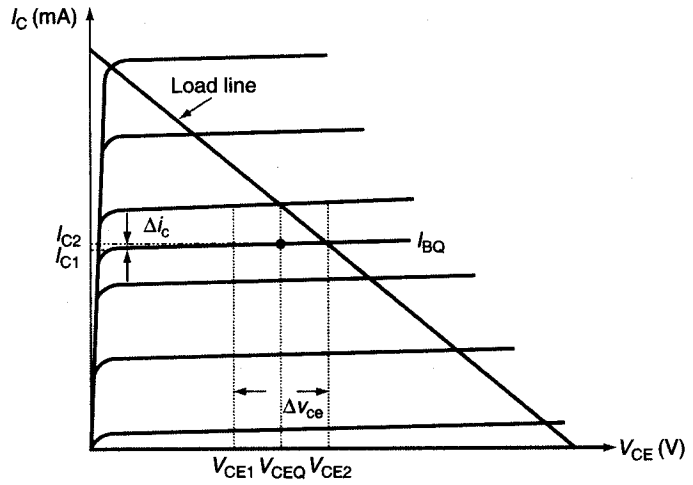


Figure 8.12 | Determination of h-parameter h_{oe}.

Table 8.2 | Typical h-parameter values for silicon transistor

Parameter	Common-emitter	Common-collector	Common-base
h_i	1–6.5 kΩ	1–6.5 kΩ	20–30 Ω
h_r	$(1.5 \times 10^{-4}) - (2.5 \times 10^{-4})$	1	$(0.1 \times 10^{-4}) - (3 \times 10^{-4})$
h_f	50–250	(–50) – (–250)	–1
h_o	5–25 μmhos	5–25 μmhos	0.02–0.5 μmhos

Typical h-parameter values of the NPN silicon transistor for the three amplifier configurations are given in Table 8.2.

8.4 Analysis of a Transistor Amplifier using Complete h-Parameter Model

Figure 8.13 shows a generalized transistor-based amplifier where the transistor is replaced by its h-parameter model. As we can see from the figure, resistor R_L is the external load and V_s is the input signal source. The important parameters of any amplifier are the current gain, input impedance, voltage gain and the output impedance. The expressions for these parameters will be derived in this section.

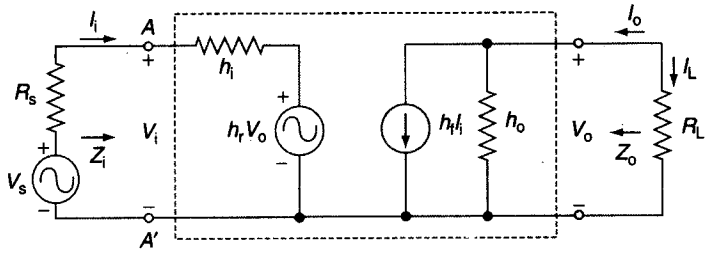


Figure 8.13 | Generalized h-parameter model of a transistor-based amplifier.

1. **Current gain or the current amplification (A_i):** Current gain is defined as the ratio of the current through the load resistance (I_L) to the input current (I_i). The following equation gives the expression for the current gain:

$$A_i = \frac{I_L}{I_i} \tag{8.21}$$

As the current $I_L = -I_o$, therefore

$$A_i = -\frac{I_o}{I_i} \tag{8.22}$$

Applying Kirchhoff's current law to the output section of the circuit shown in Figure 8.13, the value of I_o is given by

$$I_o = h_f I_i + h_o V_o \tag{8.23}$$

The value of the output voltage V_o is given by

$$V_o = I_L R_L = -I_o R_L \tag{8.24}$$

Therefore, the current gain (A_i) is given by

$$A_i = -\frac{h_f}{1 + h_o R_L} \tag{8.25}$$

This is the current gain without taking the source resistor (R_s) into account. The overall current gain taking source resistor into account can be determined by replacing the voltage source with its Norton's equivalent as shown in Figure 8.14.

The overall current gain is determined using the following expression:

$$A_{is} = -\frac{I_o}{I_s} \tag{8.26}$$

The above equation can be rewritten as

$$A_{is} = -\frac{I_o}{I_i} \times \frac{I_i}{I_s} = A_i \times \frac{I_i}{I_s}$$

The value of current I_i is given by

$$I_i = I_s \times \left(\frac{R_s}{Z_i + R_s} \right) \tag{8.27}$$

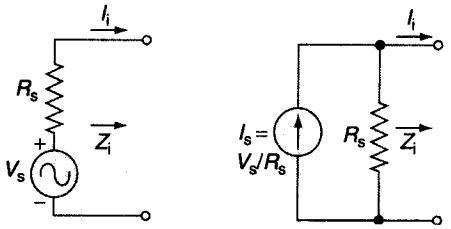


Figure 8.14 | Norton's equivalent of a voltage source.

Therefore, the overall current gain (A_{is}) is given by

$$A_{is} = A_i \times \left(\frac{R_s}{Z_i + R_s} \right) \tag{8.28}$$

From Eq. (8.28), it is clear that when $R_s \to \infty$, $A_{is} \to A_i$. Therefore, A_i is the current gain for an ideal current source.

2. **Input impedance (Z_i):** The input impedance Z_i is defined as the impedance seen looking into the input terminals A–A' of the amplifier. It is given by

$$Z_i = \frac{V_i}{I_i} \tag{8.29}$$

Applying Kirchhoff's voltage law to the input section of the amplifier we get

$$V_i = h_i I_i + h_r V_o \tag{8.30}$$

Substituting the value of V_i given by Eq. (8.30) in Eq. (8.29), we get

$$Z_i = \frac{h_i I_i + h_r V_o}{I_i} \tag{8.31}$$

The output voltage V_o is given by

$$V_o = -I_o R_L = A_i I_i R_L \tag{8.32}$$

Substituting the value of V_o in Eq. (8.31), we get

$$Z_i = \frac{h_i I_i + h_r A_i I_i R_L}{I_i} = h_i + h_r A_i R_L$$

Substituting the value of A_i given in Eq. (8.25) in the above equation we get

$$Z_i = h_i - \frac{h_r h_f R_L}{1 + h_o R_L} \tag{8.33}$$

3. **Voltage gain (A_v):** The voltage gain A_v is given by the ratio of the output voltage (V_o) to the input voltage (V_i).

$$A_v = \frac{V_o}{V_i}$$

Substituting the value of V_o given in Eq. (8.32) in the above equation, we get

$$A_v = \frac{A_i I_i R_L}{V_i} \tag{8.34}$$

Substituting the value of $V_i / I_i = Z_i$, we get

$$A_v = \frac{A_i R_L}{Z_i}$$

The voltage gain taking source resistance R_s into account (A_{vs}) is given by

$$A_{vs} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \times \frac{V_i}{V_s} = A_v \times \frac{V_i}{V_s} \tag{8.35}$$

From the equivalent input circuit of the amplifier, the voltage (V_i) is expressed in terms of the signal voltage (V_s) by

$$V_i = \frac{V_s Z_i}{Z_i + R_s} \tag{8.36}$$

Therefore, the expression for A_{vs} is given by

$$A_{vs} = \frac{A_v Z_i}{Z_i + R_s} \tag{8.37}$$

When $R_s \to 0$ then $A_{vs} \to A_v$. In other words, A_v is the voltage gain for an ideal voltage source, that is, the one with zero internal resistance.

4. **Output admittance (Y_o):** The output admittance (Y_o) is defined as the reciprocal of the output impedance (Z_o). The output impedance (Z_o) is determined by setting the voltage source (V_s) to zero and the load impedance R_L to infinity and by driving the output terminals from a voltage source (V_o). Z_o is then given by the ratio of the applied voltage (V_o) to output current (I_o).

$$Y_o = \left.\frac{I_o}{V_o}\right|_{V_s = 0, R_L = \infty} \tag{8.38}$$

Substituting the value of I_o from Eq. (8.23) in Eq. (8.38), we get

$$Y_o = h_f \frac{I_i}{V_o} + h_o \tag{8.39}$$

Applying Kirchhoff's voltage law to the input section of the circuit in Figure 8.13, we get

$$V_s - R_s I_i - h_i I_i - h_r V_o = 0 \tag{8.40}$$

As $V_s = 0$, therefore

$$R_s I_i + h_i I_i + h_r V_o = 0 \tag{8.41}$$

Rearranging the terms in Eq. (8.41), we get

$$\frac{I_i}{V_o} = -\frac{h_r}{h_i + R_s} \tag{8.42}$$

Substituting the value of I_i/V_o given by Eq. (8.42) in Eq. (8.39), we get

$$Y_o = h_o - \frac{h_f h_r}{h_i + R_s} \tag{8.43}$$

In this expression, it is assumed that the load R_L is external to the amplifier. If the effect of load resistor R_L is included, then the total impedance is given by the parallel combination of Z_o and R_L.

EXAMPLE 8.2 *For the circuit shown in Figure 8.15, determine the input impedance, voltage gain, current gain and output impedance. The values of the h-parameters of the transistor are $h_{ie} = 1.5\ k\Omega$, $h_{fe} = 100$, $h_{re} = 1 \times 10^{-4}$ and $h_{oe} = 25\ \mu A/V$.*

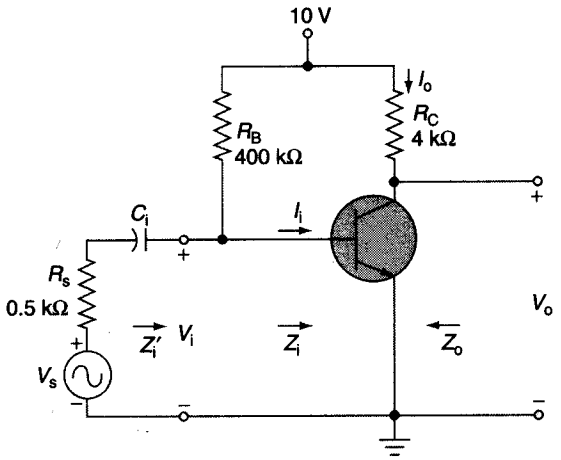
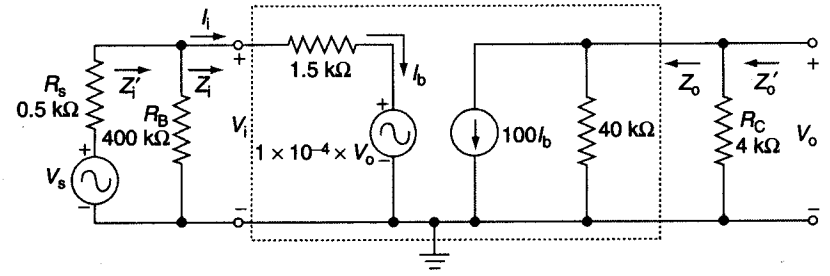


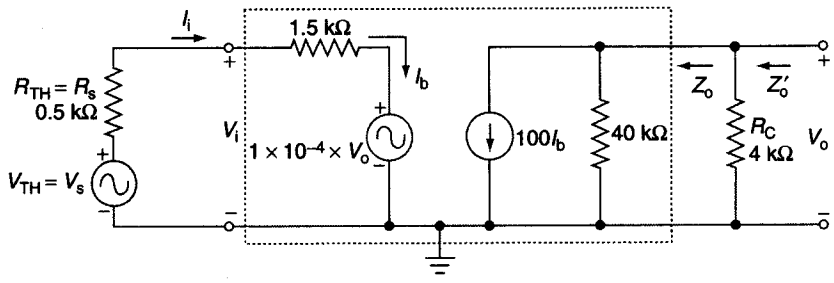
Figure 8.15 | Example 8.2.

Solution

1. The complete hybrid equivalent model for the network in Figure 8.15 is shown in Figure 8.16(a). Figure 8.16(b) shows the simplified circuit of the network shown in Figure 8.16(a) with the input section being replaced by its Thevenin's equivalent circuit.



(a)



(b)

Figure 8.16 | Solution to Example 8.2.

As the resistor $R_B >> R_s$, therefore the Thevenin's equivalent voltage V_{TH} is approximately equal to the source voltage V_s and the Thevenin's equivalent resistance R_{TH} is approximately equal to the resistor R_s.

2. The input impedance Z_i is equal to

$$Z_i = h_{ie} - \frac{h_{fe}h_{re}R_C}{1+h_{oe}R_C}$$
$$= 1.5\times10^3 - \frac{100\times1\times10^{-4}\times4\times10^3}{1+25\times10^{-6}\times4\times10^3}$$
$$= 1.5\times10^3 - \frac{40}{1.1}$$
$$= 1500 - 36.36 = 1.464\ \text{k}\Omega$$

3. The voltage gain A_v is equal to

$$A_v = \frac{V_o}{V_i} = \frac{-h_{fe}R_C}{h_{ie}+(h_{ie}h_{oe}-h_{fe}h_{re})R_C}$$
$$= \frac{-100\times4\times10^3}{1.5\times10^3+(1.5\times10^3\times25\times10^{-6}-100\times1\times10^{-4})\times4\times10^3}$$
$$= \frac{-4\times10^5}{1.5\times10^3+0.0275\times4\times10^3}$$
$$= \frac{-4\times10^5}{1.61\times10^3} = -248.45$$

4. The current gain A_i is equal to

$$A_i = -\frac{h_{fe}}{1+h_{oe}R_C}$$
$$= \frac{-100}{1+25\times10^{-6}\times4\times10^3}$$
$$= -90.91$$

5. The output impedance Z_o' is parallel combination of Z_o and R_C.

6. Z_o is given by

$$Z_o = \frac{1}{h_{oe}-[h_{fe}h_{re}/(h_{ie}+R_s)]}$$
$$= \frac{1}{25\times10^{-6}-[(100\times1\times10^{-4})/(1.5\times10^3+500)]}$$
$$= \frac{1}{25\times10^{-6}-5\times10^{-6}} = 50\ \text{k}\Omega$$

7. The overall output impedance $Z_o' = 50\times10^3 \| 4\times10^3 = 3.7\times10^3 = 3.7\ \text{k}\Omega$.

8.5 Analysis of Transistor Amplifier Configurations using Simplified h-Parameter Model

The simplified h-parameter model of a transistor was discussed in the Section 8.3. In this section, we will discuss the analysis of the various transistor amplifier configurations using the simplified h-parameter model.

Common-Emitter Configuration

The analysis for the fixed-bias configuration, voltage-divider configuration, emitter-bias configuration with unbypassed emitter resistor is discussed in the following subsections.

Fixed-Bias Configuration

Figure 8.17(a) shows the circuit diagram of the fixed-bias configuration and Figure 8.17(b) shows the simplified h-parameter equivalent model.

The input impedance Z_i is given by a parallel combination of resistor R_B and transistor's h_{ie} parameter:

$$Z_i = R_B \| h_{ie} \tag{8.44}$$

The output impedance (Z_o) is given by the parallel combination of resistor R_C and the inverse of the output admittance h-parameter h_{oe}:

$$Z_o = R_C \| (1/h_{oe}) \tag{8.45}$$

The voltage gain A_v is given by

$$A_v = \frac{V_o}{V_i} \tag{8.46}$$

The magnitude of the output voltage V_o is given by

$$V_o = -I_o Z_o = -I_c Z_o \tag{8.47}$$

The collector current (I_c) is given by

$$I_c = h_{fe} I_b \tag{8.48}$$

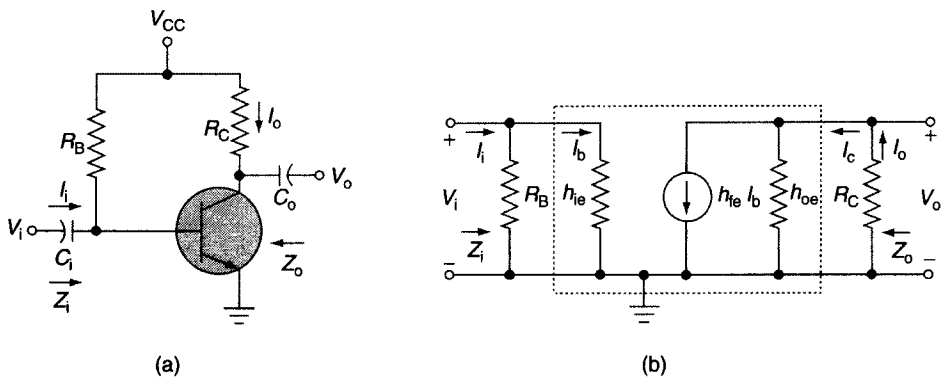


Figure 8.17 (a) Circuit diagram of fixed-bias configuration; (b) simplified h-parameter equivalent model.

The base current (I_b) in turn is expressed in terms of the input voltage V_i as

$$I_b = \frac{V_i}{h_{ie}} \tag{8.49}$$

Substituting the value of I_c given by Eq. (8.48) and value of I_b given by Eq. (8.49) in Eq. (8.47), we get

$$V_o = -h_{fe} \times \frac{V_i}{h_{ie}} \times Z_o \tag{8.50}$$

Substituting this value of V_o in the Eq. (8.46), the voltage gain is given by

$$A_v = \frac{-h_{fe} \times (V_i / h_{ie}) \times Z_o}{V_i} = \frac{-h_{fe} \times Z_o}{h_{ie}} = \frac{-h_{fe} \times [R_C \| (1/h_{oe})]}{h_{ie}} \tag{8.51}$$

The current gain A_i is given by

$$A_i = \frac{I_o}{I_i} \tag{8.52}$$

The magnitude of I_o is given by

$$I_o = I_c = h_{fe} I_b \tag{8.53}$$

Base current I_b is expressed in terms of the input current I_i as

$$I_b = \frac{R_B}{R_B + h_{ie}} \times I_i \tag{8.54}$$

Therefore, the current gain A_i is given by

$$A_i = \frac{h_{fe} I_b}{I_i} = \frac{h_{fe}}{I_i} \times \frac{R_B}{R_B + h_{ie}} \times I_i = \frac{h_{fe} \times R_B}{R_B + h_{ie}} \tag{8.55}$$

Assuming $R_B >> h_{ie}$, $A_i \cong h_{fe}$.

Voltage-Divider Configuration

Figure 8.18(a) shows the voltage-divider configuration and Figure 8.18(b) shows its h-parameter equivalent model. As we can see from the figure, the equivalent circuit is the same as in the case of fixed-bias circuit with the difference that the resistor R_B is replaced by parallel combination of resistors R_{B1} and R_{B2}. The analysis for the voltage-divider configuration is done on similar lines as that for the fixed-bias configuration.

Input impedance Z_i is given by

$$Z_i = (R_{B1} \| R_{B2}) \| h_{ie} \tag{8.56}$$

The output impedance Z_o is given by the parallel combination of resistor R_C and the inverse of the output admittance h-parameter h_{oe}:

$$Z_o = R_C \| (1 / h_{oe}) \tag{8.57}$$

The voltage gain A_v is given by

$$A_v = \frac{-h_{fe} \times [R_C \| (1 / h_{oe})]}{h_{ie}} \tag{8.58}$$

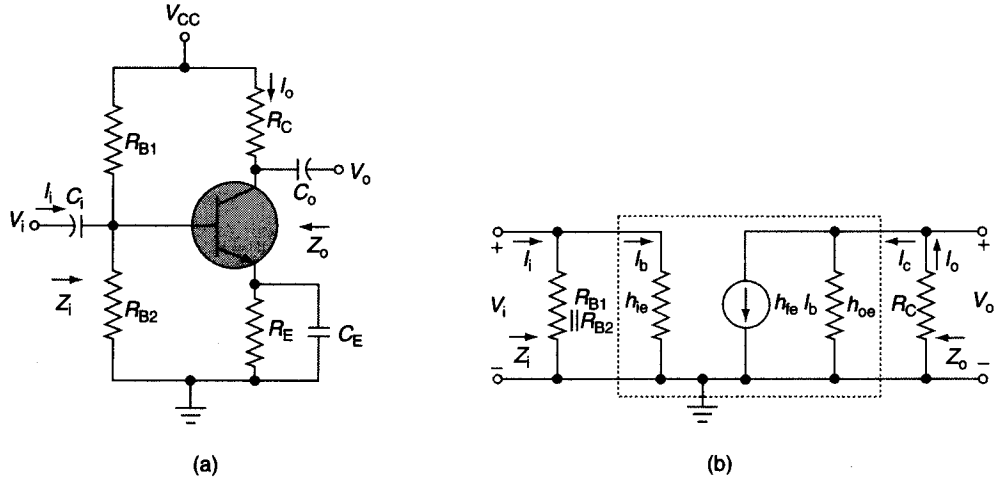


Figure 8.18 | (a) Circuit diagram of voltage-divider configuration; (b) simplified h-parameter model.

The current gain A_i is given by

$$A_i = \frac{h_{fe} \times (R_{B1} \| R_{B2})}{(R_{B1} \| R_{B2}) + h_{ie}} \tag{8.59}$$

Emitter-Bias Configuration with Unbypassed Emitter Resistor

Figure 8.19(a) shows the circuit diagram of the emitter-bias configuration with unbypassed emitter resistor and Figure 8.19(b) shows its h-parameter model representation.

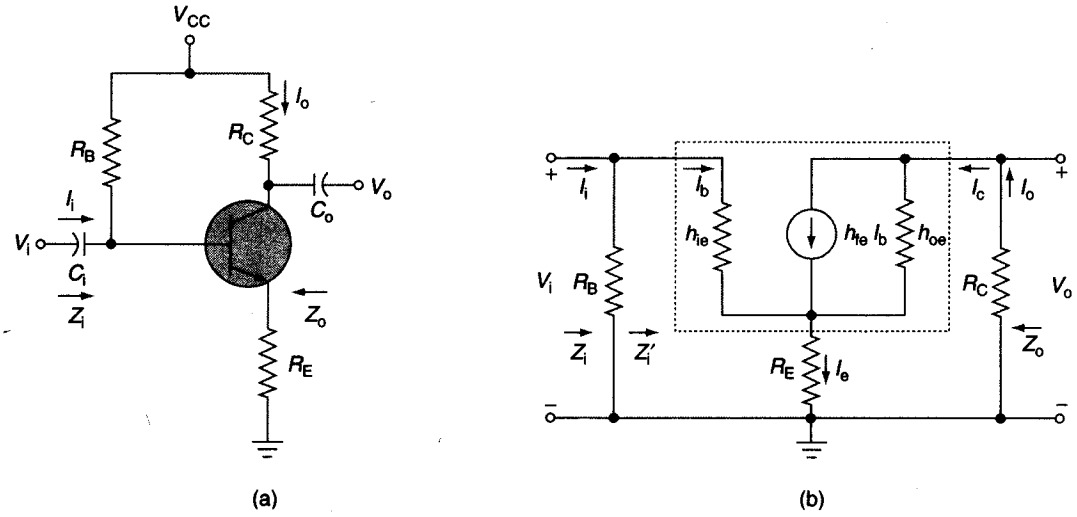


Figure 8.19 | (a) Circuit diagram of emitter-bias configuration with unbypassed emitter capacitor; (b) simplified h-parameter model.

Applying Kirchhoff's voltage law to the input section we get

$$V_i = I_b h_{ie} + I_e R_E = I_b h_{ie} + (h_{fe}+1) I_b R_E = [h_{ie} + (h_{fe}+1) R_E] I_b$$

The input impedance looking into the network to the right of resistor R_B is given by

$$Z_i' = \frac{V_i}{I_b} = h_{ie} + (h_{fe}+1) R_E \tag{8.60}$$

The overall input impedance Z_i is given by parallel combination of resistor R_B and impedance Z_i':

$$Z_i = R_B \| Z_i' \tag{8.61}$$

The voltage gain A_v is given by

$$A_v = \frac{V_o}{V_i} \tag{8.62}$$

The output voltage V_o is given by

$$V_o = -I_o R_C = -I_c R_C = -h_{fe} I_b R_C \tag{8.63}$$

The base current I_b is given by

$$I_b = \frac{V_i}{Z_i'} \tag{8.64}$$

Therefore, the magnitude of voltage gain A_v is given by

$$A_v = -\frac{h_{fe} I_b R_C}{V_i} = -\frac{h_{fe} R_C}{Z_i'} = -\frac{h_{fe} R_C}{h_{ie} + (h_{fe}+1) R_E} \tag{8.65}$$

The magnitude of current gain A_i is given by

$$A_i = \frac{I_o}{I_i} \tag{8.66}$$

The output current I_o is given by

$$I_o = I_c = h_{fe} I_b \tag{8.67}$$

The base current I_b is expressed in terms of the input current I_i as

$$I_b = \frac{R_B}{R_B + Z_i'} \times I_i \tag{8.68}$$

The value of the current gain A_i is then given by

$$A_i = \frac{h_{fe} I_b}{I_i} = \frac{h_{fe} R_B}{R_B + Z_i'} = \frac{h_{fe} R_B}{R_B + h_{ie} + (h_{fe}+1) R_E} \tag{8.69}$$

Emitter–Follower Configuration

Figure 8.20(a) shows the emitter–follower configuration and Figure 8.20(b) shows its h-parameter equivalent model.

The input impedance is determined in a similar manner as that for the emitter-bias configuration with unbypassed emitter resistor. The input impedance looking into the network to the right of resistor R_B is given by

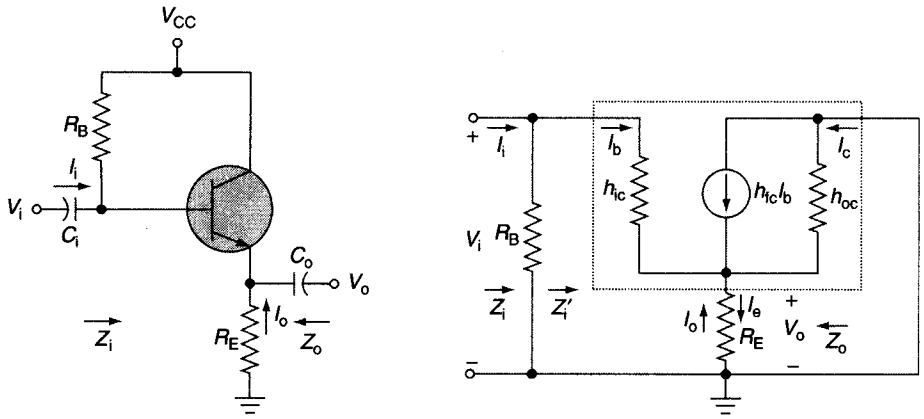


Figure 8.20 (a) Circuit diagram of emitter–follower configuration; (b) simplified h-parameter equivalent model.

$$Z_i' = \frac{V_i}{I_b} = h_{ic} - h_{fc}R_E = h_{ie} + (h_{fe}+1)R_E \tag{8.70}$$

The overall input impedance Z_i is given by parallel combination of resistor R_B and impedance Z_i':

$$Z_i = R_B \| Z_i' \tag{8.71}$$

The output impedance Z_o can be determined as follows.

The base current I_b is given by

$$I_b = \frac{V_i}{Z_i'} \tag{8.72}$$

The emitter current I_e is then given as

$$I_e = -h_{fc}I_b = (h_{fe}+1)I_b = (h_{fe}+1)\times\frac{V_i}{Z_i'} \tag{8.73}$$

Substituting the value of Z_i' in the above equation we get

$$I_e = (h_{fe}+1)\times\frac{V_i}{h_{ie}+(h_{fe}+1)R_E} = \frac{V_i}{h_{ie}/(h_{fe}+1)+R_E} \tag{8.74}$$

Figure 8.21 shows the network defined by Eq. (8.74).

The output impedance Z_o is defined by setting the input voltage V_i equal to zero. The output impedance Z_o is a parallel combination of resistor R_E and impedance defined by $h_{ie}/(h_{fe}+1)$.

$$Z_o = R_E \| [h_{ie}/(h_{fe}+1)] \tag{8.75}$$

From Figure 8.21, the output voltage V_o is expressed in terms of the input voltage V_i as

$$V_o = \frac{R_E}{R_E + h_{ie}/(h_{fe}+1)} \times V_i \tag{8.76}$$

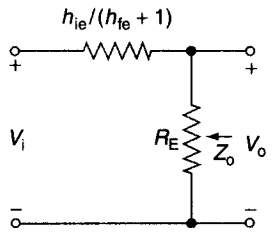


Figure 8.21 | Equivalent network.

The voltage gain A_v is then given by

$$A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + h_{ie}/(h_{fe}+1)} \tag{8.77}$$

The current gain A_i is given by

$$A_i = \frac{I_o}{I_i}$$

The output current I_o is given by

$$I_o = -I_e = h_{fc} I_b = -(h_{fe}+1) I_b$$

From Figure 8.20(b), the base current I_b is given by

$$I_b = \frac{R_B}{R_B + Z_i'} \times I_i \tag{8.78}$$

Therefore, A_i is given by

$$A_i = \frac{-(h_{fe}+1) I_b}{I_i} = \frac{-(h_{fe}+1) R_B}{R_B + Z_i'} \tag{8.79}$$

Common-Base Configuration

Figure 8.22(a) shows the circuit diagram of common-base configuration and Figure 8.22(b) shows its simplified h-parameter equivalent model.

Input impedance Z_i is given by parallel combination of resistor R_E and parameter h_{ib}:

$$Z_i = R_E \| h_{ib} = R_E \| [h_{ie}/(h_{fe}+1)] \tag{8.80}$$

The output impedance Z_o is equal to the parallel combination of collector resistor R_C and $1/h_{ob}$:

$$Z_o = R_C \| (1/h_{ob}) \cong R_C \tag{8.81}$$

The output voltage V_o is given by

$$V_o = -I_o R_C = h_{fb} I_e R_C \tag{8.82}$$

The emitter current I_e is expressed in terms of the input voltage V_i as

$$I_e = -\frac{V_i}{h_{ib}} \tag{8.83}$$

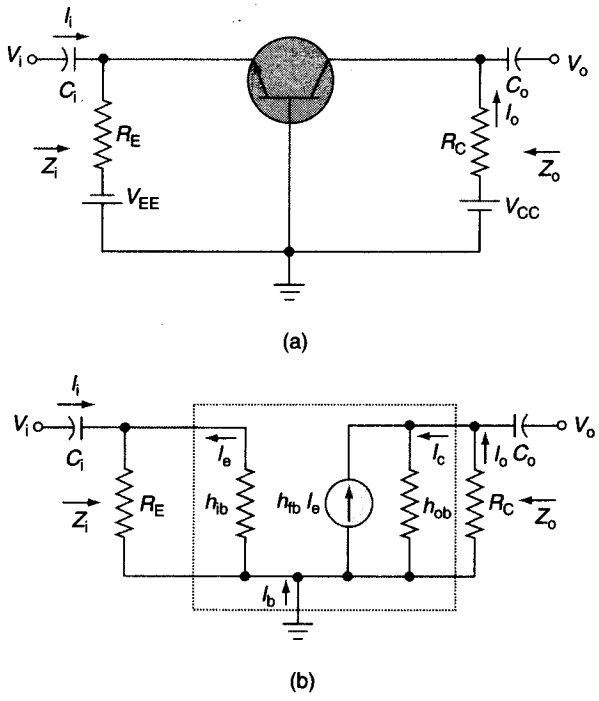


Figure 8.22 (a) Circuit diagram of common-base configuration; (b) simplified h-parameter equivalent model.

Therefore, voltage gain A_v is given by

$$A_v = \frac{V_o}{V_i} = \frac{+h_{fb} I_e R_C}{-h_{ib} I_e} = -\frac{h_{fb} R_C}{h_{ib}} = \frac{h_{fe} R_C}{h_{ie}} \tag{8.84}$$

The current gain A_i is given by

$$A_i = \frac{I_o}{I_i} = \frac{-h_{fb} I_e}{I_i} \tag{8.85}$$

The emitter current I_e is expressed in terms of the input current I_i by

$$I_e = \frac{-R_E}{R_E + h_{ib}} \times I_i \tag{8.86}$$

Therefore, current gain is given by

$$A_i = \frac{h_{fb} R_E}{R_E + h_{ib}} = \frac{h_{fb} R_E}{R_E + h_{ie}/(1 + h_{fe})} \cong h_{fb} \tag{8.87}$$

EXAMPLE 8.3 *Determine the following parameters for the amplifier shown in Figure 8.23. Given that the h-parameters of the transistor are* $h_{ie} = 1\ k\Omega$, $h_{fe} = 100$, $h_{oe} = 40 \times 10^{-6}$ *mhos.*
(a) Z_i; *(b)* Z_o; *(c)* A_v; *(d)* A_i

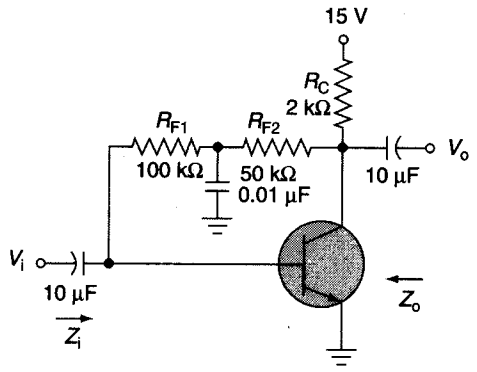


Figure 8.23 | Example 8.3.

Solution

1. The AC equivalent circuit for the amplifier in Figure 8.23 is shown in Figure 8.24.

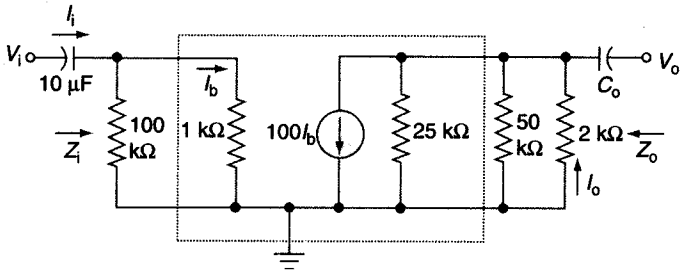


Figure 8.24 | Solution to Example 8.3.

2. Input impedance

$$\begin{aligned} Z_i &= R_{F1} \| h_{ie} \\ &= 100 \times 10^3 \| 1 \times 10^3 \\ &= 0.99 \text{ k}\Omega \end{aligned}$$

3. Output impedance (Z_o) is given by

$$\begin{aligned} Z_o &= R_{F2} \| R_C \| (1/h_{oe}) \\ &= 50 \times 10^3 \| 2 \times 10^3 \| 25 \times 10^3 \\ &= 1.79 \times 10^3 \ \Omega \\ &= 1.79 \text{ k}\Omega \end{aligned}$$

4. Voltage gain A_v is given by

$$\begin{aligned} A_v &= \frac{-h_{fe} \times [R_{F2} \| R_C \| (1/h_{oe})]}{h_{ie}} \\ &= \frac{-100 \times 1.79 \times 10^3}{1 \times 10^3} \\ &= -179 \end{aligned}$$

5. The current gain A_i is given by

$$A_i = \frac{h_{fe} R_{F1} [R_{F2} \| (1/h_{oe})]}{(R_{F1} + h_{ie}) [R_{F2} \| (1/h_{oe}) + R_C]}$$

$$= \frac{100 \times 100 \times 10^3 \times (50 \times 10^3 \| 25 \times 10^3)}{(100 \times 10^3 + 1 \times 10^3) \times (50 \times 10^3 \| 25 \times 10^3 + 2 \times 10^3)}$$

$$= \frac{10^7 \times 16.67 \times 10^3}{101 \times 10^3 \times 18.67 \times 10^3} = 88.4$$

8.6 Small Signal Analysis of FET Amplifiers

The linear small signal model for FETs can be obtained on similar lines as that for BJTs. The expression for the drain current is given by

$$I_d = V_{gs} \left. \frac{\partial i_d}{\partial v_{gs}} \right|_{V_{DS} = \text{const.}} + V_{ds} \left. \frac{\partial i_d}{\partial v_{ds}} \right|_{V_{GS} = \text{const.}} \tag{8.88}$$

The parameter g_m is defined as the transconductance or the mutual conductance and is given by

$$g_m = \left. \frac{\partial i_d}{\partial v_{gs}} \right|_{V_{DS} = \text{const.}} \tag{8.89}$$

It is also designated as y_{fs} or g_{fs} and is also referred to as forward transadmittance. The second important parameter used to define the operation of FETs is the drain resistance designated as r_d. It is defined by Eq. (8.90). The reciprocal of drain resistance r_d is referred to as the drain conductance (designated as g_d). It is also known as output conductance and is also denoted as y_{os}.

$$r_d = \left. \frac{\partial v_{ds}}{\partial i_d} \right|_{V_{GS} = \text{const.}} \tag{8.90}$$

Substituting the values of g_m given by Eq. (8.89) and r_d given by Eq. (8.90) in Eq. (8.88) we get

$$I_d = g_m V_{gs} + \frac{1}{r_d} V_{ds} \tag{8.91}$$

The amplification factor m of an FET is defined as

$$\mu = \left. \frac{\partial v_{ds}}{\partial v_{gs}} \right|_{I_D = \text{const.}} \tag{8.92}$$

The parameters g_m, r_d and m are related by the following equation:

$$\mu = r_d g_m \tag{8.93}$$

The low-frequency model of an FET is defined by Eq. (8.91) and is shown in Figure 8.25. As we can see from the figure, it has a Norton's equivalent output circuit with a voltage-dependent current source whose current output is proportional to the gate-source voltage (V_{gs}). Also, the input impedance between the gate and the source

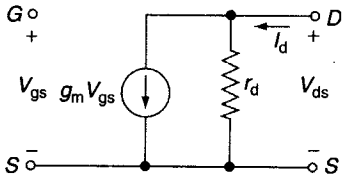


Figure 8.25 | Low-frequency model of an FET.

terminals is infinite because it is assumed that there is no current flowing through the reverse-biased gate terminal. The above equations and the model in Figure 8.25 are applicable for both JFETs as well as MOSFETs.

When we compare this model of the FET with that of the BJT, we find that there a few major differences. First, the value of the current generated by the output current source in the case of an FET depends on the input voltage whereas in the case of a BJT it depends upon the input current. Second, in the case of an FET, there is no feedback from the output to the input whereas in the case of a BJT there is feedback between the output and the input sections through parameter h_{re}. Lastly, the input impedance of an FET is much larger than that of a BJT. In nutshell, FET is more closer to being an ideal amplifier than a BJT at low frequencies.

Common-Source FET Amplifier

The common-source FET amplifier is shown in Figure 8.26(a). Replacing the FET by its low-frequency small signal model, the equivalent circuit of Figure 8.26(b) is obtained.

Applying Kirchhoff's voltage law to the output section we get

$$I_d R_D + (I_d - g_m V_{gs}) r_d = 0 \tag{8.94}$$

The voltage between the gate and the source terminals (V_{gs}) is equal to the input voltage V_i. Rearranging the terms in Eq. (8.94) and substituting $V_{gs} = V_i$, we get

$$I_d = \frac{g_m r_d V_i}{r_d + R_D} = \frac{\mu V_i}{r_d + R_D} \tag{8.95}$$

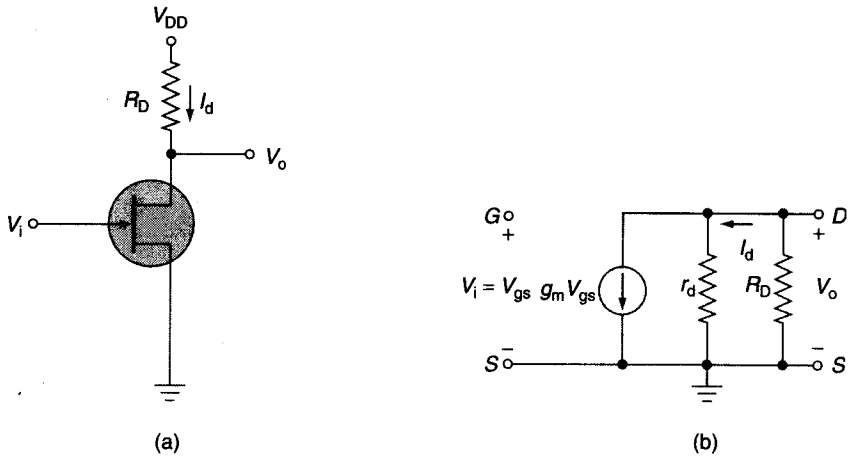


Figure 8.26 | (a) Common-source FET amplifier; (b) low-frequency small signal equivalent model of the amplifier in (a).

The output voltage V_o is given by

$$V_o = -I_d R_D = -\frac{\mu R_D V_i}{r_d + R_D} \tag{8.96}$$

Therefore, the voltage gain A_v is given by

$$A_v = \frac{V_o}{V_i} = -\frac{\mu R_D}{r_d + R_D} \tag{8.97}$$

For the common-source amplifier with an unbypassed source resistor (R_S), the analysis can be carried out on similar lines and the voltage gain is given by

$$A_v = -\frac{\mu R_D}{r_d + R_D + (\mu + 1)R_S} \tag{8.98}$$

Common-Drain FET Amplifier

The common-drain FET amplifier is shown in Figure 8.27(a). Replacing the FET by its low-frequency small signal model, the equivalent circuit of Figure 8.27(b) is obtained. The analysis is carried on similar lines to that of the common-source FET amplifier.

Applying Kirchhoff's voltage law to the output section we get

$$I_d R_S + (I_d - g_m V_{gs}) r_d = 0 \tag{8.99}$$

The gate-source voltage is expressed as

$$V_{gs} = V_i - I_d R_S \tag{8.100}$$

Combining Eqs. (8.99) and (8.100) we get

$$I_d = \frac{g_m r_d V_i}{r_d + R_S + g_m r_d R_S} = \frac{\mu V_i}{r_d + (\mu + 1)R_S} \tag{8.101}$$

The output voltage V_o is given by

$$V_o = I_d R_S = \frac{\mu R_S V_i}{r_d + (\mu + 1)R_S} \tag{8.102}$$

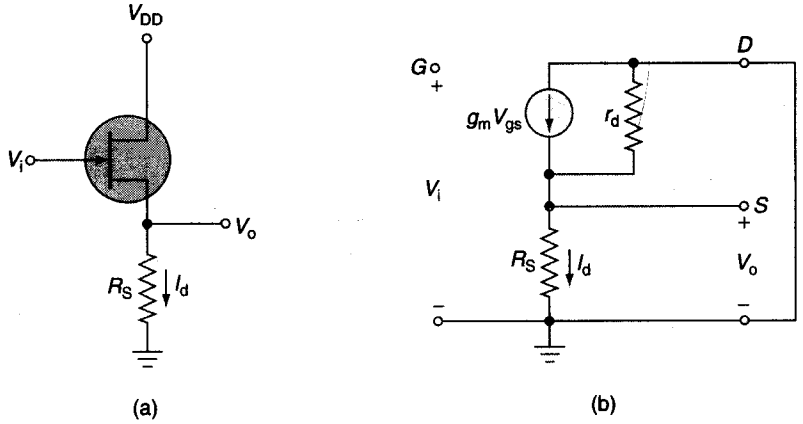


Figure 8.27 (a) Common-drain amplifier; (b) low-frequency small signal equivalent model of the amplifier in part (a).

Therefore, the voltage gain A_v is given by

$$A_v = \frac{V_o}{V_i} = \frac{\mu R_S}{r_d + (\mu + 1)R_S} \tag{8.103}$$

For the common-drain amplifier with an unbypassed drain resistor (R_D), the analysis can be carried out on similar lines and the voltage gain is given by

$$A_v = \frac{\mu R_S}{r_d + R_D + (\mu + 1)R_S} \tag{8.104}$$

As the value of μ is very large, therefore the term $(\mu + 1)R_S >> (r_d + R_D)$. Therefore, Eq. (8.104) can by approximated as

$$A_v \cong \frac{\mu R_S}{(\mu + 1)R_S} \cong \frac{\mu}{\mu + 1} \cong 1 \tag{8.105}$$

EXAMPLE 8.4

For the self-bias JFET amplifier shown in Figure 8.28, determine the value of (a) Z_i, (b) Z_o and (c) A_v. Given that $I_{DSS} = 10$ mA, $V_p = -5$ V and $r_d = 50$ kΩ. The quiescent operating point is $V_{GSQ} = -2.5$ V and $I_{DQ} = 2.5$ mA.

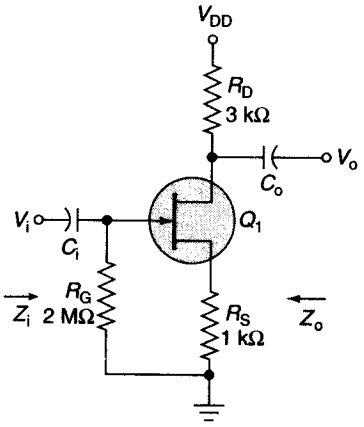


Figure 8.28 | Example 8.4.

Solution

1. Figure 8.29 shows the equivalent circuit for the amplifier in Figure 8.28.
2. The input impedance (Z_i) is given by $Z_i = R_G$. Therefore, $Z_i = 2$ MΩ.
3. The output impedance can be calculated as

$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i = 0}$$

4. For $V_i = 0$, the output voltage V_o is defined by $V_o = -I_d R_D$ and the gate-source voltage (V_{gs}) is defined by $V_{gs} = -I_d R_S$.
5. For $V_i = 0$, the current through resistor r_d is equal to

$$I' = \frac{V_{rd}}{r_d} = \frac{V_o + V_{gs}}{r_d} = \frac{-I_d(R_D + R_S)}{r_d}$$

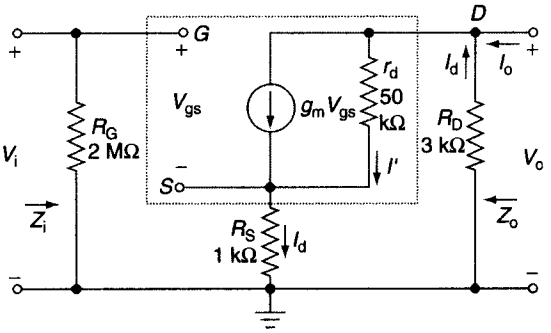


Figure 8.29 | Solution to Example 8.4.

6. Applying KCL at the drain node (D), $I_d + I_o = I' + g_m V_{gs}$.
7. Therefore,

$$I_o = -I_d\left(1 + g_m R_S + \frac{R_D + R_S}{r_d}\right)$$

8. Therefore, Z_o is given by

$$Z_o = \frac{R_D}{1 + g_m R_S + [(R_D + R_S)/r_d]}$$

9. The value of g_m is given by

$$g_m = g_{mo}\left(1 - \frac{V_{GSQ}}{V_P}\right)$$

10.
$$g_{mo} = \frac{2I_{DSS}}{|V_P|}$$
$$= \frac{2 \times 10 \times 10^{-3}}{5}$$
$$= 4 \text{ mS}$$

11. Therefore, $g_m = 4 \times 10^{-3}\,[1 - (-2.5)/(-5)] = 2$ mS
12. Output impedance Z_o is given by

$$Z_o = 3 \times 10^3/[1 + 2 \times 10^{-3} \times 1 \times 10^3 + (3 \times 10^3 + 1 \times 10^3)/(50 \times 10^3)]$$
$$= (3 \times 10^3)/(3 + 0.08) = 0.97 \text{ k}\Omega$$

13. The value of voltage gain A_v can be calculated as follows:

Applying KVL to the input section we get $V_{gs} = V_i - I_d R_S$

14. Applying KCL to the drain node (D) we get

$$I_d = g_m V_{gs} + \frac{V_o - V_{RS}}{r_d}$$

15. Output voltage V_o is equal to $V_o = -I_d R_D$.

16. Therefore, I_d is given by

$$I_d = \frac{g_m V_i}{1 + g_m R_S + [(R_D + R_S)/r_d]}$$

17. Voltage gain A_v is equal to

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + [(R_D + R_S)/r_d]}$$
$$= \frac{-2\times10^{-3}\times3\times10^3}{1 + 2\times10^{-3}\times1\times10^3 + [(3\times10^3 + 1\times10^3)/(50\times10^3)]}$$
$$= -1.95$$

8.7 Cascading Amplifiers

Many times, the gain of a single-amplifier stage is not sufficient for the intended application or the input or the output impedance of the amplifier is not of the correct magnitude for the given application. In such cases, two or more amplifier stages are cascaded, that is, the output of a given stage is connected to the input of the next amplifier stage. A cascade connection of amplifiers is a series connection where the output of one stage is applied to the input of the next stage. As an example, the common-emitter amplifier is used for cascading to provide power gain, common-collector amplifier may be used as the last stage to drive a low-resistance load as it has low output resistance or it may be used as first stage of the amplifier by virtue of its high input impedance.

Figure 8.30 shows a generalized cascaded amplifier connection. The total gain is the product of the gains of the individual amplifier stages under loaded conditions. The overall gain (A_v) is therefore given by

$$A_v = A_{v1} \times A_{v2} \times A_{v3} \times \cdots \times A_{vn} \tag{8.106}$$

where A_v is the overall voltage gain; A_{v1} is the voltage gain of stage 1 with the input impedance of stage 2 acting on it; A_{v2} is the voltage gain of stage 2 with the input impedance of stage 3 acting on it and its source impedance is the output impedance of stage 1; A_{v3} is the voltage gain of stage 3 with the input impedance of stage 4 acting on it and its source impedance is the output impedance of stage 2; A_{vn} is the voltage gain of stage n with the load impedance acting on it and its source impedance is the output impedance of stage $(n-1)$.

The overall current gain is given by

$$A_i = -A_v \times \left(\frac{Z_{il}}{R_L}\right) \tag{8.107}$$

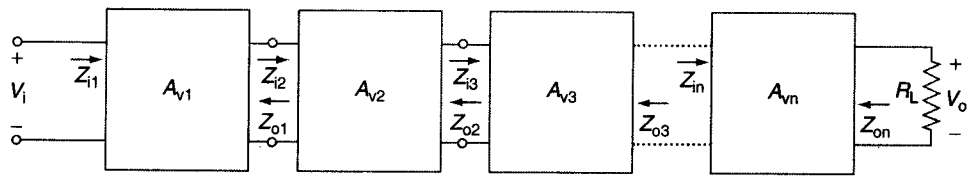


Figure 8.30 Generalized cascaded amplifier connection.

where A_i is the overall current gain; A_v is the overall voltage gain; Z_{i1} is the input impedance of the stage 1; R_L is the load resistance.

It may be mentioned here that the DC bias conditions for the cascaded amplifier stages can be determined on similar lines as that discussed in Chapter 4 for BJT amplifiers and in Chapter 5 for FET amplifiers.

EXAMPLE 8.5

Figure 8.31 shows a two-stage CC-CB amplifier. The values of input and output impedances and the voltage gains for each stage are shown in the figure. All the values are for no-load conditions. However, the input impedance and the output impedance of the first stage are under loaded conditions. Determine

(a) The loaded voltage gain for each stage.

(b) The overall voltage gain of the amplifier.

(c) The total system voltage and current gain.

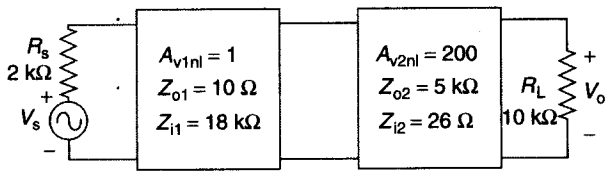


Figure 8.31 | Example 8.5.

Solution

1. The loaded voltage gain of the second-stage, that is, the CB amplifier is given by

$$A_{v2} = A_{v2nl} \times [R_L/(R_L + Z_{o2})]$$
$$= 200 \times [(10 \times 10^3)/(10 \times 10^3 + 5 \times 10^3)]$$
$$= 133.33$$

2. The loaded voltage gain of the first stage, that is, the CC amplifier is given by

$$A_{v1} = A_{v1nl} \times [Z_{i2}/(Z_{i2} + Z_{o1})] = 1 \times [26/(26 + 10)] = 26/36 = 0.722$$

3. The overall voltage gain of the amplifier $= A_{v1} \times A_{v2} = 0.722 \times 133.33 = 96.26$.

4. The value of total system voltage gain

$$A_{vs} = A_v \times [Z_{i1}/(Z_{i1} + R_s)] = 96.26 \times [(18 \times 10^3)/(18 \times 10^3 + 2 \times 10^3)]$$
$$= -86.63$$

5. The value of the total system current gain

$$A_{is} = -(A_{vs} \times Z_{i1})/R_L = -(86.63 \times 18 \times 10^3)/(10 \times 10^3) = -155.93$$

BJT Cascade Amplifier

Figure 8.32 shows a cascaded three-stage RC-coupled BJT amplifier. Let the h-parameters of the transistor Q_1 be h_{ie1}, h_{fe1}, h_{re1} and h_{oe1}; of transistor Q_2 be h_{ie2}, h_{fe2}, h_{re2} and h_{oe2} and that of transistor Q_3 be h_{ie3}, h_{fe3}, h_{re3} and h_{oe3}.

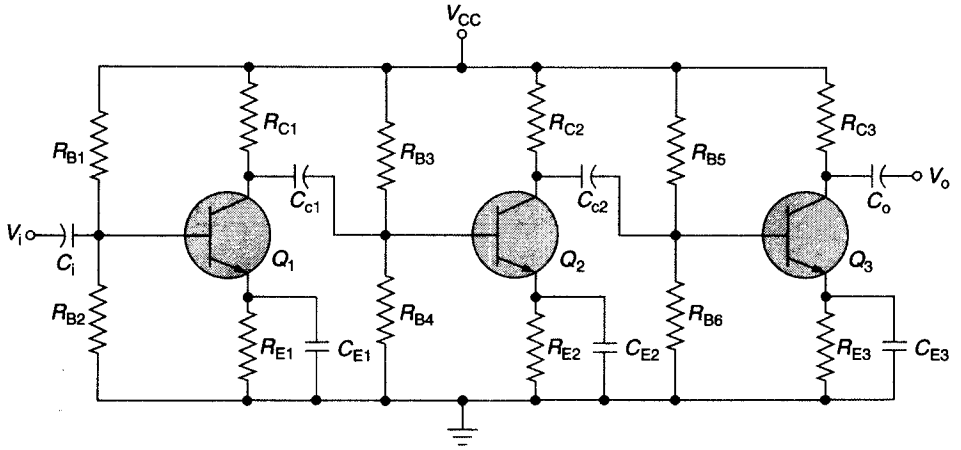


Figure 8.32 | Cascaded three-stage RC-coupled BJT amplifier.

The voltage gain of the third stage is given by

$$A_{v3} = \frac{-h_{fe3} \times [R_{C3} \| (1/h_{oe3})]}{h_{ie3}} \tag{8.108}$$

Assuming $1/h_{oe} >> R_{C3}$, the equation can be simplified as

$$A_{v3} = \frac{-h_{fe3} \times R_{C3}}{h_{ie3}} \tag{8.109}$$

Similarly, the gain for the second stage A_{v2}, assuming $1/h_{oe2} >> R_{B5} \| R_{B6} \| R_{C2} \| h_{ie3}$ is given by

$$A_{v2} = \frac{-h_{fe2} \times (R_{B5} \| R_{B6} \| R_{C2} \| h_{ie3})}{h_{ie2}} \tag{8.110}$$

The gain for the first stage A_{v1}, assuming $1/h_{oe1} >> R_{B3} \| R_{B4} \| R_{C1} \| h_{ie2}$ is given by

$$A_{v1} = \frac{-h_{fe1} \times (R_{B3} \| R_{B4} \| R_{C1} \| h_{ie2})}{h_{ie1}} \tag{8.111}$$

The overall voltage gain A_v is given by the product of the voltage gains of the three stages:

$$A_v = A_{v1} \times A_{v2} \times A_{v3} \tag{8.112}$$

The overall input impedance of the amplifier is the same as the input impedance of stage 1 and is given by

$$Z_i = R_{B1} \| R_{B2} \| h_{ie1} \tag{8.113}$$

The output impedance of the amplifier is equal to the output impedance of the last stage and is given by

$$Z_o = R_{C3} \| (1/h_{oe3}) \tag{8.114}$$

EXAMPLE 8.6

Figure 8.33 shows a two-stage BJT cascaded amplifier. Calculate the voltage gain, input and output impedance of the amplifier, given that h_{ie} and h_{fe} parameters of both the transistors are 1 kΩ and 100, respectively. Assume that the effect of h_{oe} is negligible.

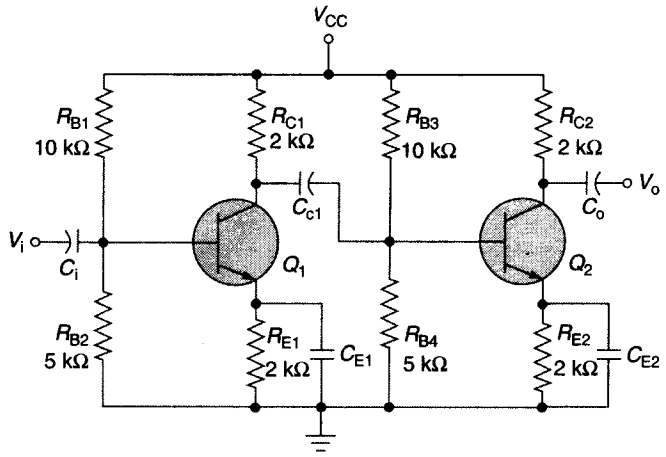


Figure 8.33 | Example 8.6.

Solution

1. Voltage gain of the second stage is given by

$$A_{v2} = \frac{-h_{fe2} \times R_{C2}}{h_{ie2}}$$

$$= \frac{-100 \times 2 \times 10^3}{1 \times 10^3} = -200$$

2. Voltage gain of the first stage is given by

$$A_{v1} = \frac{-h_{fe1} \times (R_{B3} \| R_{B4} \| R_{C1} \| h_{ie2})}{h_{ie1}}$$

$$= \frac{-100 \times (10 \times 10^3 \| 5 \times 10^3 \| 2 \times 10^3 \| 1 \times 10^3)}{1 \times 10^3}$$

$$= \frac{-100 \times 555.56}{1 \times 10^3} = -55.556$$

3. Overall voltage gain is given by $A_v = A_{v1} \times A_{v2} = -200 \times -55.556 = 11111.2$.

4. The input impedance of the amplifier Z_i is given by

$$Z_i = R_{B1} \| R_{B2} \| h_{ie1}$$

$$= 10 \times 10^3 \| 5 \times 10^3 \| 1 \times 10^3 = 769.05\ \Omega$$

5. The output impedance of the amplifier is given by $Z_o = R_{C2} \| (1/h_{oe2})$. As the effect of h_{oe} is negligible, therefore $Z_o = R_{c2} = 2$ kΩ.

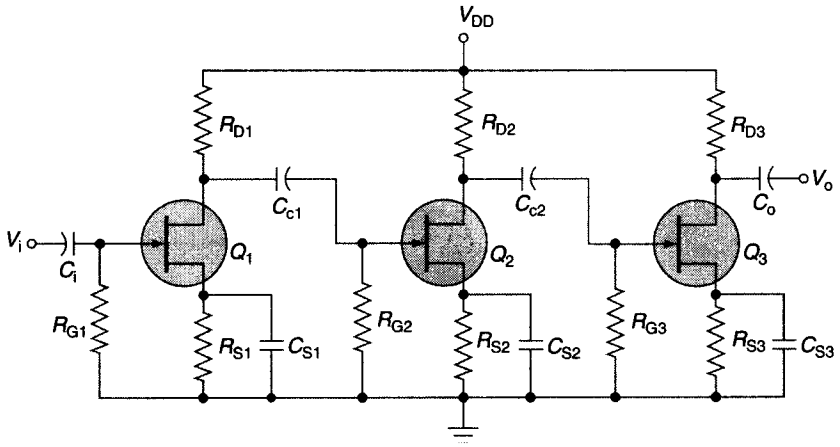


Figure 8.34 | Cascaded three-stage RC-coupled JFET amplifier.

FET Cascade Amplifier

Figure 8.34 shows a cascaded three-stage RC-coupled JFET amplifier. The gains of the first, second and third stages are given respectively by the following three equations:

$$A_{v1} = -g_{m1}R_{D1} \tag{8.115}$$

$$A_{v2} = -g_{m2}R_{D2} \tag{8.116}$$

$$A_{v3} = -g_{m3}R_{D3} \tag{8.117}$$

where R_{D1}, R_{D2} and R_{D3} are the drain resistors for stage-1, stage-2 and stage-3 amplifiers respectively; g_{m1}, g_{m2} and g_{m3} are the transconductance values for the stage-1, stage-2 and stage-3 amplifiers, respectively. The overall gain A_v is given by

$$A_v = A_{v1} \times A_{v2} \times A_{v3} \tag{8.118}$$

The input impedance Z_i of the cascaded amplifier is the same as the input impedance of the stage 1:

$$Z_i = R_{G1} \tag{8.119}$$

The output impedance Z_o is given by the output impedance of the last stage:

$$Z_o = R_{D3} \tag{8.120}$$

A combination of FET and BJT stages can also be used to provide both high value of voltage gain as well as high value of input impedance.

EXAMPLE 8.7 | *Figure 8.35 shows a two-stage cascaded amplifier with the first stage as a common-source JFET amplifier and the second stage as a common-emitter BJT amplifier. Calculate the voltage gain, input and output impedances of the amplifier. Given that h_{ie} and h_{fe} parameters of the transistor are 1 kΩ and 100, respectively. Assume that the effect of h_{oe} is negligible. The transconductance g_m of the JFET is 2.6 mS.*

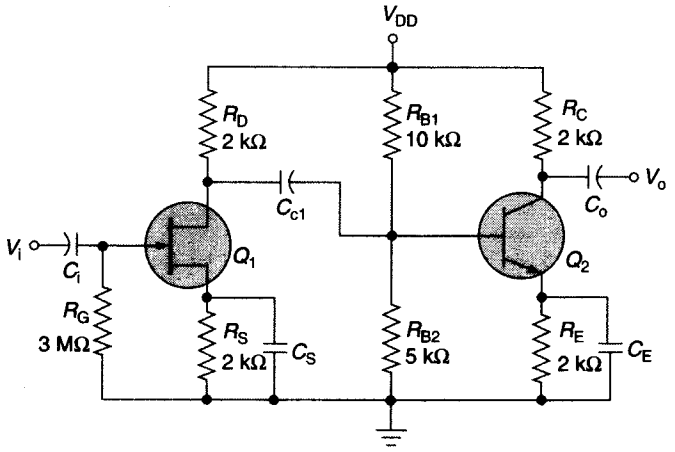


Figure 8.35 | Example 8.7.

Solution

1. Voltage gain of the second stage is given by

$$A_{v2} = \frac{-h_{fe} \times R_C}{h_{ie}}$$

$$= \frac{-100 \times 2 \times 10^3}{1 \times 10^3} = -200$$

2. Voltage gain of the first stage is given by

$$A_{v1} = -g_m (R_D \| R_{B1} \| R_{B2} \| h_{ie})$$

$$= -2.6 \times 10^{-3} \times (2 \times 10^3 \| 10 \times 10^3 \| 5 \times 10^3 \| 1 \times 10^3)$$

$$= -2.6 \times 10^{-3} \times 555.56 = -1.45$$

3. Overall voltage gain is given by $A_v = A_{v1} \times A_{v2} = -200 \times -1.45 = 290$.
4. The input impedance of the amplifier Z_i is given by $Z_i = R_G$. Therefore, $Z_i = 3$ MΩ.
5. The output impedance of the amplifier is given by $Z_o = R_C \| (1/h_{oe})$. As the effect of h_{oe} is negligible, therefore $Z_o = R_C = 2$ kΩ.

8.8 Darlington Amplifiers

Darlington transistors refer to the connection of two BJTs wherein their collector terminals are tied together and the emitter terminal of one of the transistors is connected to the base terminal of the other transistor. In other words, the Darlington connection can be considered as two cascaded emitter–followers, with the first stage having an infinite emitter resistance. The composite transistor acts as a single unit (Figure 8.36) with a current gain approximately equal to the product of the current gains of the individual transistors. If the individual transistors have current gains of β_1 and β_2, then the Darlington connection provides an approximate current gain of β_D given by

$$\beta_D = \beta_1 \times \beta_2 \tag{8.121}$$

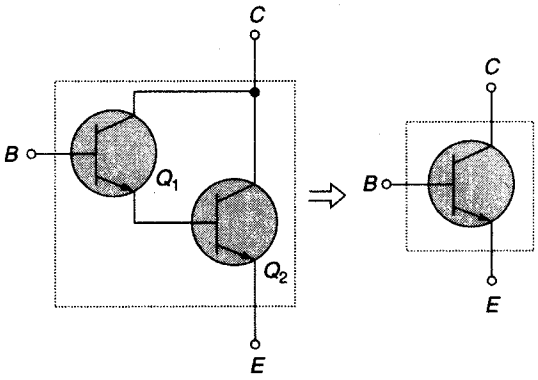


Figure 8.36 | Darlington transistor.

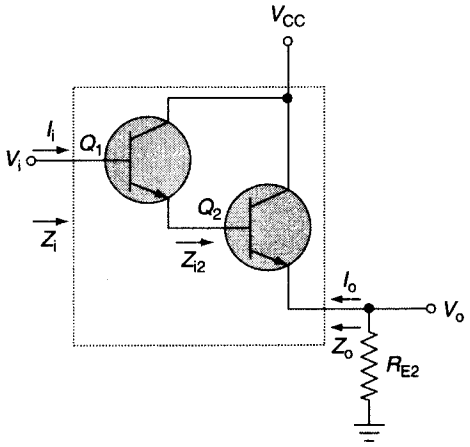


Figure 8.37 | Circuit using a Darlington transistor.

It offers other advantages like increased value of input impedance and reduced value of output impedance. The values of these parameters are derived in the subsequent paragraphs. Figure 8.37 shows a circuit configuration employing a Darlington pair. The biasing network for Q_1 has not been included for simplicity of analysis. The current gain for the second transistor Q_2 is given by

$$A_{i2} = \frac{I_o}{I_{b2}} = \frac{1+h_{fe2}}{1+h_{oe2}R_{E2}} \cong 1+h_{fe2} \tag{8.122}$$

The input resistance of the second stage is given by

$$Z_{i2} = h_{ie2} + (1+h_{fe2})R_{E2} \cong (1+h_{fe2})R_{E2} \tag{8.123}$$

Z_{i2} is the effective load resistance for the first-stage Q_1 and the current gain for the first stage (A_{i1}) is given by

$$\begin{aligned} A_{i1} &= \frac{I_{e1}}{I_i} = \frac{I_{b2}}{I_i} = \frac{1+h_{fe1}}{1+h_{oe1}Z_{i2}} \\ &\cong \frac{1+h_{fe1}}{1+h_{oe1}(1+h_{fe2})R_{E2}} \\ &\cong \frac{1+h_{fe1}}{1+h_{oe1}h_{fe2}R_{E2}} \end{aligned} \tag{8.124}$$

The overall current gain (A_i) is given by

$$A_i = \frac{I_o}{I_i} = \frac{I_o}{I_{b2}} \times \frac{I_{b2}}{I_i} = A_{i2} \times A_{i1} \cong (1+h_{fe2})\left(\frac{1+h_{fe1}}{1+h_{oe1}h_{fe2}R_{E2}}\right) \tag{8.125}$$

Assuming that the h-parameters for both the transistors are equal, that is, $h_{fe1} = h_{fe2} = h_{fe}$ and $h_{oe1} = h_{oe2} = h_{oe}$, the above equation can be rewritten as

$$A_i \cong \left(\frac{(1+h_{fe})^2}{1+h_{oe}h_{fe}R_{E2}}\right) \tag{8.126}$$

The overall voltage gain (A_v) is less than unity, because it consists of two emitter–followers in cascade, each offering value of voltage gain slightly less than unity.

$$A_v = \frac{V_o}{V_i} \cong \left(1 - \frac{h_{ie}}{Z_{i2}}\right) \tag{8.127}$$

The overall input impedance (Z_i) is given by

$$Z_i = \frac{A_i R_{E2}}{A_v} \cong A_i R_{E2} \cong \frac{(1+h_{fe})^2 R_{E2}}{1+h_{oe}h_{fe}R_{E2}} \tag{8.128}$$

The output impedance (Z_o) is given by

$$Z_o \cong \frac{R_s + h_{ie}}{(1+h_{fe})^2} + \frac{h_{ie}}{1+h_{fe}} \tag{8.129}$$

where R_s is the value of the source resistance.

In deriving the above equations, we have omitted the biasing network for transistor Q_1 to simplify the analysis. The biasing network mainly affects the input impedance of the amplifier. Figure 8.38(a) shows the biasing arrangement. Let us now consider the effect of the biasing network of transistor Q_1 on the input impedance of the network.

The overall input impedance (Z_i') is given by

$$Z_i' = Z_i \| R \tag{8.130}$$

where $R = R_{B1} \| R_{B2}$. The value of R (i.e., parallel combination of R_{B1} and R_{B2}) is much less than the value of Z_i. Therefore, the overall input impedance (Z_i') is appreciably smaller than Z_i. This nullifies one of the major advantages offered by a Darlington amplifier of high input impedance.

This can be partially overcome by adding a resistor R_{B3} as shown in Figure 8.38(b). The new value of R is now

$$R = R_{B1} \| R_{B2} + R_{B3} \tag{8.131}$$

The value of R is still less than Z_i. The value of R can be substantially improved if we add a capacitor C_B in addition to resistor R_{B3} [Figure 8.38(c)]. The reactance of the capacitor is negligible at low frequencies at which the amplifier is to be used. Hence, the capacitor (C_B) directly couples the output voltage V_o to the lower side of resistor R_{B3}. The other end of the resistor R_{B3} is connected to the input voltage V_i. As the

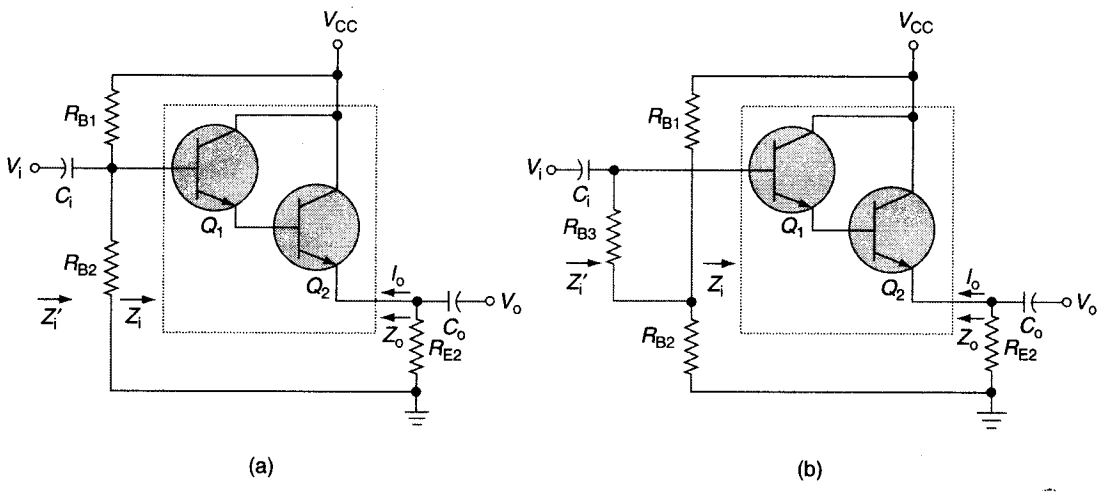
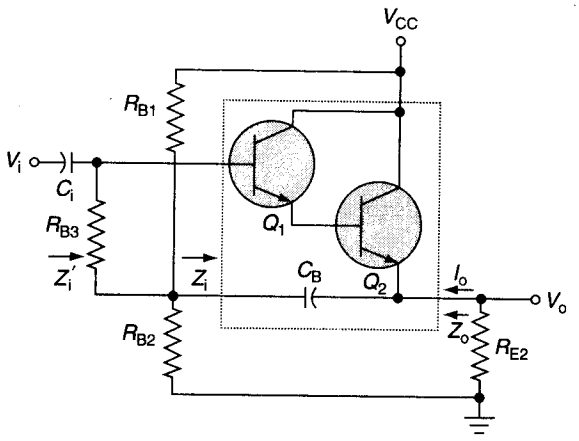


Figure 8.38 (a) Darlington amplifier with input bias circuit; (b) Darlington amplifier with modified input bias circuit; (c) bootstrapping in Darlington amplifier.



(c)

Figure 8.38 | *Continued.*

voltage gain of the amplifier is nearly unity, the input voltage V_i is approximately equal to the output voltage V_o. Therefore, there is very small AC voltage drop across the resistor R_{B3}. Hence, it draws a very small AC current from the input voltage V_i. Therefore, the effective value of R_{B3} has increased manifold. The effective value of R_{B3} can be calculated by making use of Miller's effect:

$$R_{B3(eff)} = \frac{R_{B3}}{1 - A_v} \tag{8.132}$$

As the value of voltage gain (A_v) is close to unity, value of $R_{B3(eff)}$ is very large. The effect of the voltage gain (A_v) approaching unity on the resistor $R_{B3(eff)}$ is referred to as bootstrapping. For unity value of A_v both ends of R_{B3} increase by the same potential as if R_{B3} were pulling it by its bootstraps.

EXAMPLE 8.8

Figure 8.39 shows a Darlington amplifier. The two transistors Q_1 and Q_2 are identical and the h-parameters for both the transistors are h_{ie} = 1 kΩ, h_{fe} = 100 and h_{oe} = 40 × 10^{-6} mhos. The values of the voltages V_{CC} = 15 V, V_{BE1} = 0.7 V and V_{BE2} = 0.7 V. Determine the following:

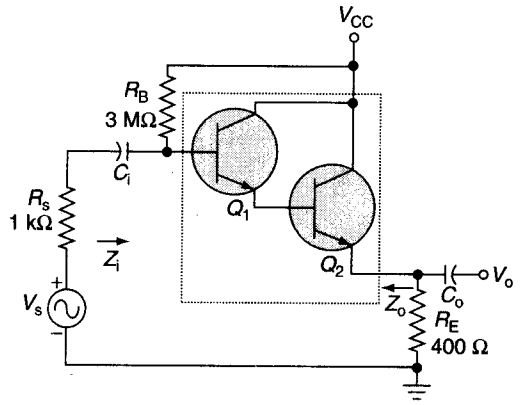


Figure 8.39 | Example 8.8.

(a) Quiescent values of DC voltages and currents.
(b) Input impedance.
(c) Output impedance.
(d) Voltage gain.
(e) Current gain.

Solution

1. The base bias current of the Darlington amplifier I_B is given by

$$I_B = \frac{V_{CC} - V_{BE1} - V_{BE2}}{R_B + (1+h_{fe})^2 R_E}$$
$$= \frac{15 - 0.7 - 0.7}{3\times10^6 + (101)^2 \times 400}$$
$$= \frac{13.6}{3\times10^6 + 4.08\times10^6} = 1.92\,\mu A$$

2. Emitter current of the Darlington amplifier is

$$I_{E2} = (1 + h_{fe})^2 I_{B1} = (101)^2 \times 1.92 \times 10^{-6}\,\mu A = 19.6\text{ mA}$$

3. The collector current of the Darlington amplifier $I_C \cong I_E = 19.6$ mA.

4. The collector–emitter voltage $V_{CE} = V_C - V_E = 15 - 19.6\times10^{-3}\times400 = 7.16$ V.

5.
$$Z_i = R_B \left\| \frac{(1+h_{fe})^2 R_E}{1 + h_{oe} h_{fe} R_E} \right.$$
$$= 3\times10^6 \left\| \frac{(101)^2 \times 400}{1 + 40\times10^{-6}\times100\times400} \right.$$
$$= 3\times10^6 \| 1.57\times10^6 = 1.03\text{ M}\Omega$$

6.
$$Z_o \cong \frac{R_s + h_{ie}}{(1+h_{fe})^2} + \frac{h_{ie}}{1+h_{fe}}$$
$$= \frac{1\times10^3 + 1\times10^3}{(101)^2} + \frac{1\times10^3}{101}$$
$$= 0.196 + 9.9$$
$$= 10.1\,\Omega$$

7. Voltage gain A_v is given by

$$A_v = 1 - \frac{h_{ie}}{(1+h_{fe})R_E}$$
$$= 1 - \frac{1\times10^3}{101\times400}$$
$$= 1 - 0.025$$
$$= 0.975$$

8. Current gain A_i is given by

$$A_i = \frac{R_B}{Z_i' + R_B} \times \left(\frac{(1+h_{fe})^2}{1 + h_{oe} h_{fe} R_E} \right)$$

$$Z_i' = \frac{(1+h_{fe})^2 R_E}{1+h_{oe}h_{fe}R_E} = 1.57\times10^6$$

Therefore, A_i is given by

$$A_i = \frac{3\times10^6}{3\times10^6+1.57\times10^6}\times\frac{(101)^2}{1+40\times10^{-6}\times100\times400}$$
$$= 0.66\times3923.46 = 2589.49$$

8.9 Cascode Amplifiers

Cascode amplifiers are two-stage amplifiers comprising a transconductance amplifier followed by a current buffer. They offer advantages like high input–output isolation, high input impedance and high output impedance. In a BJT cascode amplifier configuration, the common-emitter transistor amplifier is followed by a common-base transistor amplifier. Figure 8.40(a) shows the circuit diagram of a cascode amplifier wherein the transistor Q_1 is configured as common-emitter amplifier and Q_2 is configured as common-base amplifier. The common-base amplifier Q_2 offers large bandwidth but its input impedance is low. Because of the low input impedance of Q_2, the voltage gain of Q_1 is low. Therefore, the Miller's component of capacitance of transistor Q_1 is small and the bandwidth of the cascode amplifier is wider than that for the common-emitter stage. Hence, cascode amplifiers are used for high-frequency applications.

In the case of an FET-based cascode amplifier, common-source amplifier is followed by common-gate amplifier as shown in Figure 8.40(b).

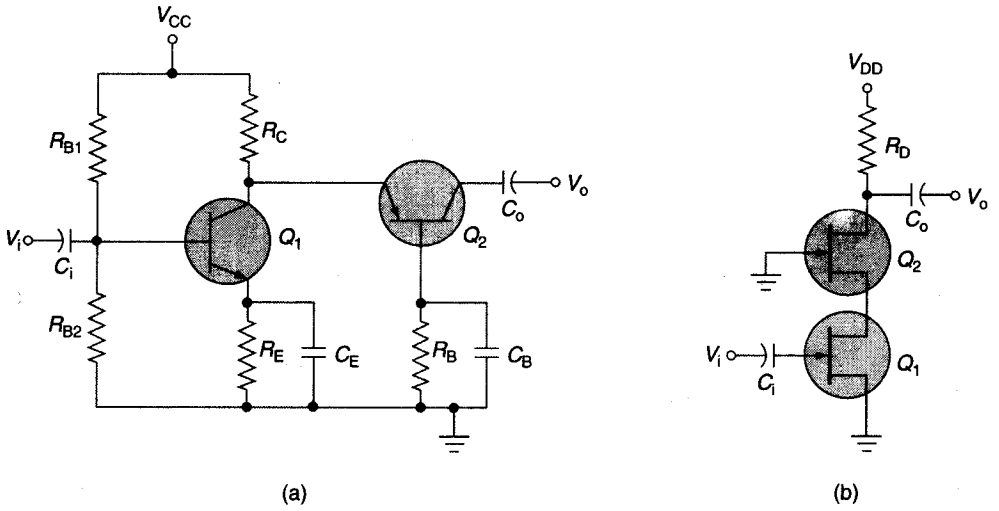


Figure 8.40 | (a) BJT cascode amplifier; (b) FET cascode amplifier.

EXAMPLE 8.9 | *For the cascode amplifier circuit shown in Figure 8.41, determine the values of resistors R_E, R_1 and R_2 such that the operating point is I_{CQ} = 10 mA and V_{CEQ} = 10 V. Given that the value of β = 100 and V_{BE} of each transistor is 0.7 V.*

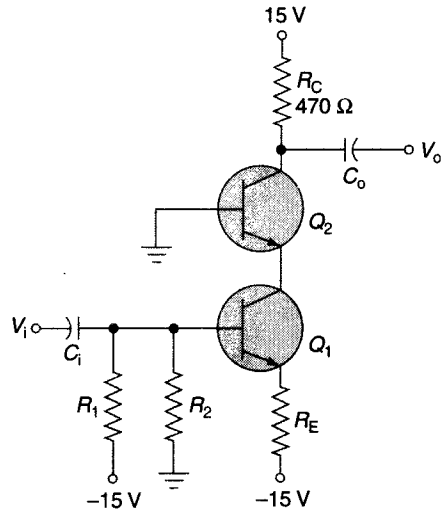


Figure 8.41 | Example 8.9.

Solution

1. DC voltage drop across the resistor R_C is given by $470 \times 10 \times 10^{-3} = 4.7$ V.
2. Therefore, the voltage drop across the resistor R_E is $15 - 4.7 - 10 - 10 - (-15) = 30 - 24.7 = 5.3$ V.
3. Value of resistor R_E is approximately equal to $5.3/10 \times 10^{-3} = 530\ \Omega$.
4. Voltage at the base of transistor Q_1 is given by $-15 + 5.3 + 0.7 = -9$ V.
5. For good bias stability, current through resistor $R_2 >> I_{BQ1}$. Value of R_2 should not be so large such that this condition is not met and also it should not be too small to have an undue load on the power supply.
6. Assume $R_2 = 10$ kΩ. Current through R_2 is $9/(10 \times 10^3) = 0.9$ mA.
7. Current through resistor $R_1 = 0.9 \times 10^{-3} - 10 \times 10^{-3}/100 = 0.9 \times 10^{-3} - 10 \times 10^{-5} = 0.89 \times 10^{-3} = 0.89$ mA.
8. Voltage drop across R_1 is $15 - 9 = 6$ V.
9. Value of resistor $R_1 = 6/(0.89 \times 10^{-3}) = 6.74$ kΩ.

8.10 Low-Frequency Response of Amplifiers

As discussed in the earlier part of the chapter, the frequency of the applied input signal has a great effect on the response of the amplifier. The low-frequency response is limited by the coupling and the bypass capacitors as they can no longer be considered as short circuits. The high-frequency response is affected by the stray capacitive elements associated with the active device. Moreover, as the number of amplifier stages increases, the low- and the high-frequency response gets further limited. In this section, we will discuss the low-frequency response of the BJT and FET amplifiers. This is followed by a discussion on the effect of cascading amplifier stages on the overall frequency response of the amplifier in the next section. The high-frequency response of amplifiers is discussed in Chapter 9.

Low-Frequency *Response of BJT Amplifiers*

In the low-frequency region of operation, a BJT or an FET amplifier's response is affected by the R–C combinations formed by the network capacitors including the coupling and bypass capacitors and the network resistive elements. In this section we discuss the effect of these capacitors on the low-frequency response of the voltage-divider BJT amplifier configuration. The results can be generalized to any transistor configuration. Figure 8.42 shows the voltage-divider BJT amplifier configuration. C_i is the input-coupling capacitor and is connected between the applied input source and the active device. C_o is the output-coupling capacitor and is connected between the output of the active device and the load.

Effect of Input Coupling Capacitor

The capacitor C_i forms an RC network as shown in Figure 8.43. R_i is the input resistance of the amplifier as seen by the source and is given by parallel combination of R_1, R_2 and h_{ie}:

$$R_i = R_1 \| R_2 \| h_{ie} \tag{8.133}$$

The voltage V_i applied to the input of the active device is calculated by using the voltage-divider rule. Therefore, voltage V_i is given by

$$V_i = \frac{R_i}{R_s + R_i - jX_{C_i}} \times V_s \tag{8.134}$$

At mid- and high frequencies the reactance of capacitors C_i and C_o will be sufficiently small to permit a short-circuit approximation. Therefore, the input voltage at mid-band frequencies ($V_{i\text{-mid}}$) is given by

$$V_{i\text{-mid}} = \frac{R_i}{R_s + R_i} \times V_s \tag{8.135}$$

The cut-off frequency established by the capacitor C_i is given by

$$f_{LC_i} = \frac{1}{2\pi(R_i + R_s)C_i} \tag{8.136}$$

At f_{LC_i} the voltage V_i will be 0.707 times the voltage $V_{i\text{-mid}}$ assuming that C_i is the only capacitive element effecting the low-frequency response.

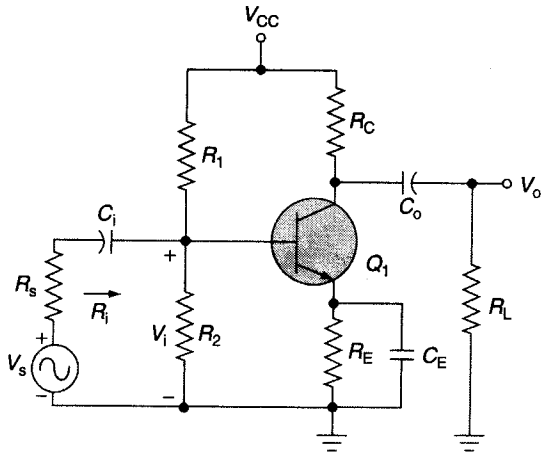


Figure 8.42 Voltage-divider BJT amplifier configuration.

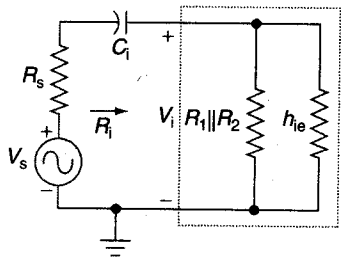


Figure 8.43 Determining the effect of input-coupling capacitor on the low-frequency response.

Effect of the Output Coupling Capacitor

The output coupling capacitor (C_o) is connected between the output of the active device and the load. Figure 8.44 shows the simplified configuration highlighting the effect of C_o on the low-frequency response of the amplifier. R_o is the total output resistance and is given by

$$R_o = R_C \| r_o \cong R_C \tag{8.137}$$

The cut-off frequency as established by C_o is given by

$$f_{LC_o} = \frac{1}{2\pi(R_o + R_L)C_o} \cong \frac{1}{2\pi(R_C + R_L)C_o} \tag{8.138}$$

The output voltage V_o will be 70.7% of its mid-band value at the frequency f_{LC_o} assuming that C_o is the only capacitive element controlling the low-frequency response.

Effect of Bypass Capacitor

Figure 8.45 shows the network as seen by the bypass capacitor C_E. The value of the equivalent resistance R_E is given by

$$R_e = R_E \| [(R_s' + h_{ie})/h_{fe}] \tag{8.139}$$

where

$$R_s' = R_s \| R_1 \| R_2$$

The cut-off frequency as established by resistance R_E and capacitor C_E is given by

$$f_{LC_E} = \frac{1}{2\pi R_e C_E} \tag{8.140}$$

The effect of bypass capacitor C_E can be explained qualitatively by considering that at low frequencies the capacitor C_E acts like an open circuit and whole of the resistor R_E appears in the gain equation, resulting in minimum value of gain. As the frequency increases, the reactance of the capacitor C_E decreases resulting in decrease in the value of parallel impedance of resistor R_E and capacitor C_E. The gain is maximum when the impedance of the capacitor C_E reduces so much that it can be considered as a short circuit.

It may be mentioned here that the input and the output coupling capacitors and the bypass capacitors effect only the low-frequency response. At the mid-band frequency range they are considered as short-circuit equivalent and do not affect the gain at these frequencies. If the cut-off frequencies offered by them are far apart then the highest cut-off frequency due to the three capacitors essentially determines the cut-off frequency of the entire system. If the cut-off frequencies are near to each other then the effect will be to raise

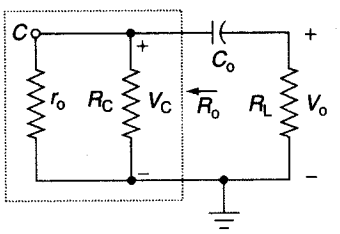


Figure 8.44 Determining the effect of output coupling capacitor on the low-frequency response.

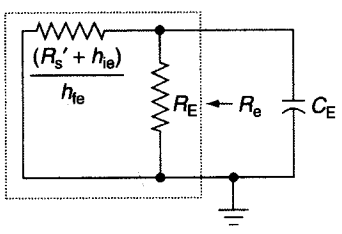


Figure 8.45 Determining the effect of bypass capacitor on the low-frequency response.

the lower cut-off frequency of the entire system, that is, there is an interaction between the capacitive elements resulting in increased lower cut-off frequency for the entire system.

Low-Frequency Response of FET Amplifiers

The low-frequency response of FET amplifiers is quite similar to that of BJT amplifiers discussed in the preceding subsection. In the case of FET amplifiers also, there are three capacitors that affect the low-frequency response, namely, the coupling capacitor C_i between the source and the FET, the coupling capacitor C_o between the FET and the load and the source capacitor C_S. Figure 8.46 shows the circuit of a JFET-based amplifier. In this section, we will discuss the effect of all the three capacitors on the low frequency response for the amplifier. The fundamental equations and the procedure apply to other amplifier configurations as well.

Effect of Input Coupling Capacitor

Figure 8.47 shows the equivalent network seen by the input coupling capacitor C_i. The cut-off frequency as determined by the capacitor C_i is given by

$$f_{LC_i} = \frac{1}{2\pi(R_i + R_s)C_i} \cong \frac{1}{2\pi(R_G + R_s)C_i} \tag{8.141}$$

In most of the applications, the value of resistor R_G is much larger than the value of the resistor R_s. Therefore, the low cut-off frequency (f_{LC_i}) is primarily determined by the values of resistor R_G and capacitor C_i.

Effect of Output Coupling Capacitor

Figure 8.48 shows the network as seen by the output coupling capacitor. The output resistance (R_o) is determined by

$$R_o = R_D \| r_d \tag{8.142}$$

The resulting cut-off frequency f_{LC_o} is given by

$$f_{LC_o} = \frac{1}{2\pi(R_o + R_L)C_o} = \frac{1}{2\pi(R_D \| r_d + R_L)C_o} \tag{8.143}$$

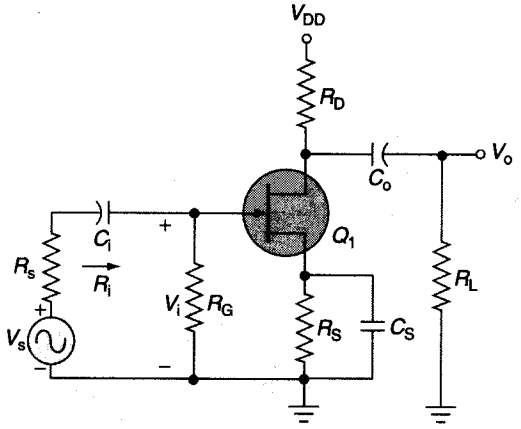


Figure 8.46 | JFET-based amplifier.

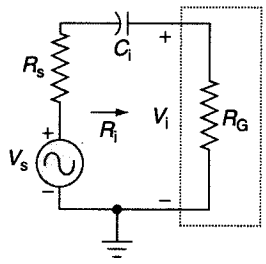


Figure 8.47 | Determining the effect of input coupling capacitor on the low-frequency response.

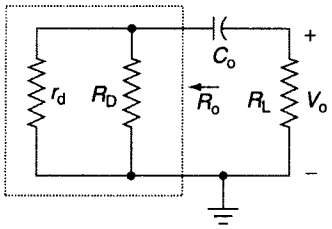


Figure 8.48 Determining the effect of output coupling capacitor on the low-frequency response.

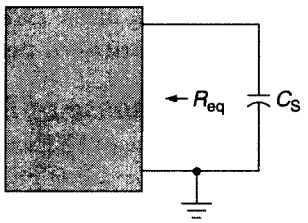


Figure 8.49 Determining the effect of source capacitor on the low-frequency response.

Effect of Source Capacitor

The equivalent network seen by the source capacitor C_S is shown in Figure 8.49. The equivalent resistance as seen by the capacitor C_S is given by

$$R_{eq} = \frac{R_S(r_d + R_D \| R_L)}{R_S(1 + g_m r_d) + r_d + R_D \| R_L} \tag{8.144}$$

As the value of resistance r_d is very large, assuming $r_d = \infty$ we get

$$R_{eq} = R_S \| (1/g_m) \tag{8.145}$$

The cut-off frequency due to the capacitor C_S is defined as

$$f_{LC_S} = \frac{1}{2\pi R_{eq} C_S} \tag{8.146}$$

EXAMPLE 8.10 *Determine the lower cut-off frequency of the BJT amplifier shown in Figure 8.50. Sketch the frequency response using Bode plot. Given that the h-parameters of the transistor are $h_{ie} = 1.5$ kΩ and $h_{fe} = 100$.*

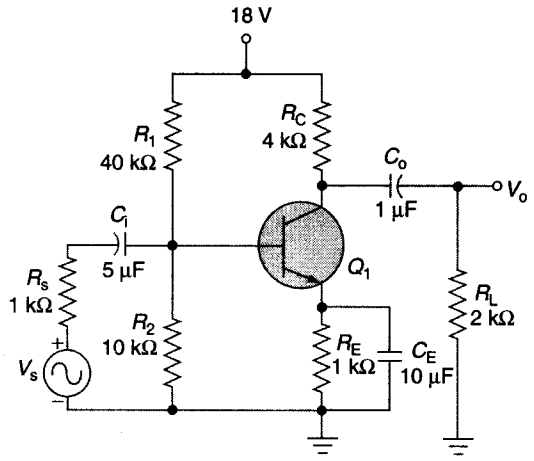


Figure 8.50 Example 8.10.

Solution

1. The cut-off frequency due to the capacitor C_i is given by

$$f_{LC_i} = \frac{1}{2\pi(R_i + R_s)C_i}$$

$$R_i = R_1 \| R_2 \| h_{ie}$$

$$= 40\times10^3 \| 10\times10^3 \| 1.5\times10^3$$

$$= 1.26\times10^3 = 1.26\ \text{k}\Omega$$

Therefore $f_{LC_i} = 1/2 \times \pi \times (1.26 \times10^3 + 1 \times 10^3) \times 5 \times 10^{-6} = 14.08$ Hz.

2. The cut-off frequency due to capacitor C_E is given by

$$f_{LC_E} = \frac{1}{2\pi R_e C_E}$$

3. $$R_e = R_E \| [(R_s \| R_1 \| R_2 + h_{ie})/h_{fe}]$$

$$= 1\times10^3 \| [(1\times10^3 \| 40\times10^3 \| 10\times10^3 + 1.5\times10^3)/100]$$

$$= 23.33\ \Omega$$

4. Therefore $f_{LC_E} = 1/2 \times \pi \times (23.33) \times 10 \times 10^{-6} = 682$ Hz.
5. The cut-off frequency due to capacitor C_o is given by

$$f_{LC_o} = \frac{1}{2\pi(R_C + R_L)C_o}$$

$$= \frac{1}{2\pi(4\times10^3 + 2\times10^3)\times1\times10^{-6}}$$

$$= 26.53\ \text{Hz}$$

6. As we can see f_{LC_E} is significantly higher than f_{LC_o} and f_{LC_i}, hence f_{LC_E} is the predominant factor in determining the low-frequency response for the complete system.
7. Hence the cut-off frequency for the overall system is approximately equal to 682 Hz.
8. Figure 8.51 shows the asymptotic curves using the Bode plot.

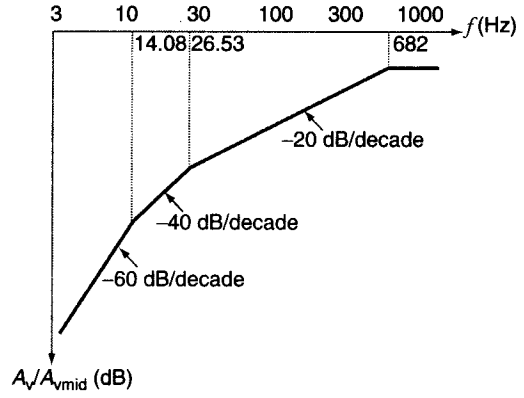


Figure 8.51 | Solution to Example 8.10.

8.11 Low-Frequency Response of Cascaded Amplifier Stages

The overall frequency response of an amplifier changes if an additional stage is added to it. In a multi-stage amplifier, the lower cut-off frequency is determined by the stage having the highest value of the lower cut-off frequency and the upper cut-off frequency is determined by the stage having the lowest value of the upper cut-off frequency. This also results in reduction of the overall bandwidth of the amplifier. The effect of adding additional stages can be best understood by considering that all stages are identical with the same lower and upper cut-off frequencies. Let the lower cut-off frequency and upper cut-off frequency of each stage be f_L and f_H, respectively. The drop-off rate in the low- and the high-frequency regions for each stage is −6 dB/octave or −20 dB/decade.

For a two-stage amplifier, the drop-off rates increase to −12 dB/octave or −40 dB/decade. The lower cut-off frequency (f_L') where the amplitude falls by 3 dB is given by

$$f_L' = \frac{f_L}{\sqrt{2^{1/2}-1}} = \frac{f_L}{0.64} = 1.56 f_L \tag{8.147}$$

The upper cut-off frequency f_H' is given by

$$f_H' = f_H\sqrt{2^{1/2}-1} = 0.64 f_H \tag{8.148}$$

Figure 8.52 shows the response of the two-stage amplifier with each stage having a unity gain. The asymptotic response is shown in Figure 8.52(a) whereas the actual response is shown in Figure 8.52(b). Also the response of single-stage amplifiers is shown to highlight the effect of cascading the two stages.

The above discussion can be generalized for n stages. Let the gain of each individual stage in the mid frequency region be A_{vmid} and the gain in the low-frequency region be A_{vlow}. Let the overall mid-frequency gain be $A_{vmid\text{-}overall}$ and the overall low-frequency gain be $A_{vlow\text{-}overall}$. Also, the lower and the upper cut-off frequencies for the individual stages are f_L and f_H, respectively, and the lower and the upper cut-off frequencies for the overall amplifier are f_{Ln} and f_{Hn}, respectively. Therefore,

$$A_{vmid\text{-}overall} = (A_{vmid})^n \tag{8.149}$$

$$A_{vlow\text{-}overall} = (A_{vlow})^n \tag{8.150}$$

Taking the ratio of Eq. (8.149) and (8.150) we get

$$\frac{A_{vlow\text{-}overall}}{A_{vmid\text{-}overall}} = \left(\frac{A_{vlow}}{A_{vmid}}\right)^n \tag{8.151}$$

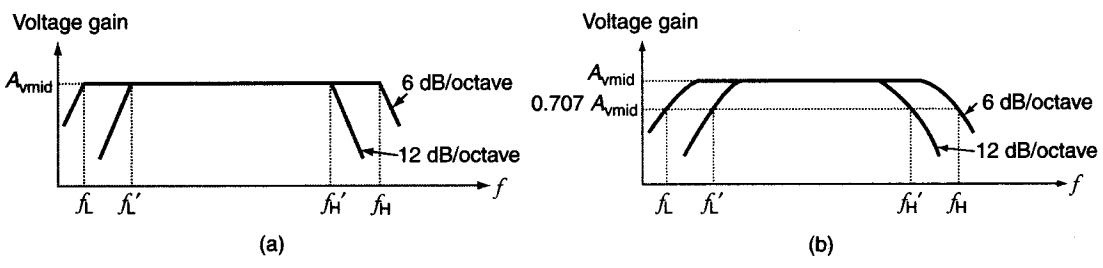


Figure 8.52 | (a) Asymptotic response of a two-stage amplifier; (b) actual response of a two-stage amplifier.

$$\frac{A_{v\text{low-overall}}}{A_{v\text{mid-overall}}} = \left(\frac{1}{(1 - jf_L/f)}\right)^n \tag{8.152}$$

Let the frequency at which the magnitude of the expression given by Eq. (8.152) become $1/\sqrt{2}$ (-3 dB) be f_{Ln}. Therefore,

$$\frac{1}{\sqrt{[1+(f_L/f_{Ln})^2]^n}} = \frac{1}{\sqrt{2}} \tag{8.153}$$

On solving Eq. (8.153), we get

$$f_{Ln} = \frac{f_L}{\sqrt{2^{1/n} - 1}} \tag{8.154}$$

Similarly, the overall upper cut-off frequency (f_{Hn}) is given by

$$f_{Hn} = f_H\sqrt{2^{1/n} - 1} \tag{8.155}$$

It may be mentioned here that increase in the number of stages is not always associated with decrease in the bandwidth. If the value of mid-band gain is kept fixed and independent of the number of amplifier stages then the bandwidth may increase with increase in the number of stages.

KEY TERMS

Cascade amplifier
Cascode amplifier
Darlington amplifier
h-parameter model
Open-circuit output admittance parameter (h_{22})
Open-circuit reverse transfer voltage ratio (h_{12})
Short-circuit forward transfer current ratio (h_{21})
Short-circuit input impedance parameter (h_{11})

OBJECTIVE-TYPE EXERCISES

Multiple-Choice Questions

1. The parameter h_{oe} can be determined by
   a. taking the slope of the output characteristic curve at the operating point.
   b. taking the slope of the input characteristic curve at the operating point.
   c. cannot be determined using the input and output characteristic curves.
   d. by taking the collector current increment for a fixed value of collector–emitter voltage.
2. What is the unit of the output conductance parameter?
   a. Ohms
   b. It is dimensionless
   c. Mhos
   d. Ampere
3. Increase in the value of transistor's h_{fe} parameter results in
   a. decrease in the value of input impedance and increase in the value of current gain.
   b. decrease in the values of both the input impedance and the current gain.
   c. increase in the values of both the input impedance and the current gain.
   d. increase in the value of input impedance and decrease in the value of current gain.

4. Increase in the junction temperature of a transistor results in
   a. increase in the values of all the four h-parameters.
   b. decrease in the values of all the four h-parameters.
   c. increase in the values of h_{ie} and h_{fe} parameters and decrease in the values of h_{re} and h_{oe} parameters.
   d. decrease in the values of h_{ie} and h_{fe} parameters and increase in the values of h_{re} and h_{oe} parameters.

5. Which of the following statement(s) is/are true?
   a. The low-frequency response of an amplifier is due to the bypass and the coupling capacitors.
   b. The high-frequency response of an amplifier is due to the bypass and the coupling capacitors.
   c. The low-frequency response of an amplifier is due to the junction capacitances and the stray-wiring capacitances.
   d. The high-frequency response of an amplifier is due to the junction capacitances and the stray-wiring capacitances.
   e. Both (a) and (d).
   f. Both (b) and (c).

6. The voltage gain of an amplifier decreases at 20 dB/decade above 100 kHz. If the mid-band frequency gain is 80 dB, what is the value of the voltage gain at 2 MHz?
   a. 60 dB
   b. 52 dB
   c. 54 dB
   d. 64 dB

7. In the h-parameter model, the input and the output sections are modeled as
   a. voltage sources.
   b. current sources.
   c. input section as voltage source and output section as current source.
   d. input section as current source and output section as voltage source.

8. Larger the spacing between the curves of the output characteristics of a transistor
   a. smaller is the value of h_{fe}.
   b. larger is the value of h_{fe}.
   c. h_{fe} is independent of the spacing.
   d. h_{fe} can increase or decrease depending upon the circuit configuration.

9. Which of the following statement(s) is/are true?
   a. In the case of an FET amplifier, there is no feedback from the output to the input whereas in the case of a BJT amplifier there is feedback between the output and the input circuits through the parameter h_{re}.
   b. In the case of a BJT amplifier, there is no feedback from the output to the input whereas in the case of an FET amplifier there is feedback between the output and input sections through the parameter g_m.
   c. BJT is a more ideal amplifier as compared to an FET.
   d. FET is a more ideal amplifier as compared to a BJT.
   e. Both (a) and (d).
   f. Both (b) and (c).

10. Which of the following statement(s) is/are false?
    a. The parameters h_i and h_r are determined from the input characteristic curves of the transistors whereas the parameters h_f and h_o are determined from the output or the collector characteristics.
    b. Cascode amplifiers are two-stage amplifiers comprising a transconductance amplifier followed by a current buffer.
    c. Darlington connection refers to the connection of two bipolar junction transistors wherein their collector terminals are tied together and the emitter terminal of one transistor is connected to the base terminal of the other transistor.
    d. Darlington connection refers to the connection of two bipolar junction transistors wherein their emitter terminals are tied together and the collector terminal of one transistor is connected to the base terminal of the other transistor.

Fill in the Blanks

1. For a multistage amplifier, the lower cut-off frequency will be determined by the stage having the _____ lower cut-off frequency and the upper cut-off frequency is determined by the stage having the _____ upper cut-off frequency.
2. The low-frequency response is limited by the _____ and the _____ capacitors while the high frequency response is affected by the _____ capacitive elements associated with the active device.
3. Darlington connection can be considered as two cascaded _____, with the first stage having an _____ emitter resistance.
4. The parameter h_{11} is the ratio of the instantaneous change in the _____ voltage due to instantaneous change in the _____ current and has the units _____.
5. The low-frequency model of an FET has a _____ output circuit with a dependent current source whose current output is proportional to the _____.

REVIEW QUESTIONS

1. Draw the frequency response of an RC-coupled amplifier and a DC-coupled amplifier. Also explain the main difference between the response of the two amplifiers.
2. Draw the comprehensive h-parameter model of a transistor. Also draw the approximate h-parameter model, highlighting the assumptions made in drawing it.
3. Derive the expressions for the voltage and current gains, input and output impedances of a collector-to-base feedback common-emitter amplifier configuration using simplified h-parameter equivalent model.
4. Why are Darlington transistors also referred to as superbeta transistors? Explain the concept using the internal schematic of Darlington transistors.
5. Explain the effect of coupling and bypass capacitors on the low-frequency response of the transistor-based amplifier.
6. Explain the effect of cascading amplifier stages on the overall frequency response of the amplifier.
7. Derive the expression for the cut-off frequencies due to the bypass and the coupling capacitors for the common-collector configuration.
8. What are cascode amplifiers? What are the advantages offered by the cascode amplifiers?
9. How can we determine the h-parameters of a transistor using its input and output characteristics curves?
10. Derive the relationship between the h_{fe} parameter of the three amplifier configurations using bipolar transistors.

PROBLEMS

1. Figure 8.53 shows a two-stage cascaded amplifier with the first stage as a common-emitter BJT amplifier and the second stage as a common-source JFET amplifier. Calculate the values of voltage gain, input and output impedances of the amplifier. Given that h_{ie} and h_{fe} parameters of the transistor are 1.2 kΩ and 120, respectively. Assume that the effect of h_{oe} is negligible. The transconductance g_m of the JFET is 3 mS.

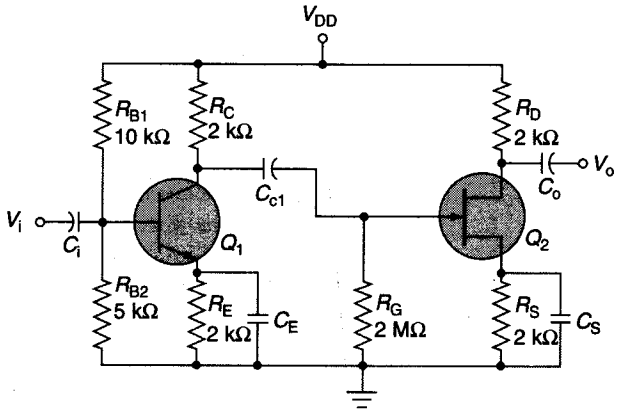


Figure 8.53 | Problem 1.

2. For the voltage-divider JFET amplifier shown in Figure 8.54, determine the value of the following parameters:

a. Z_i
b. Z_o
c. A_v

Given that the values of the FET parameters $I_{DSS} = 10$ mA, $V_p = -5$ V and $r_d = 50$ kΩ. The quiescent operating point is $V_{GSQ} = -2.5$ V and $I_{DQ} = 2.5$ mA.

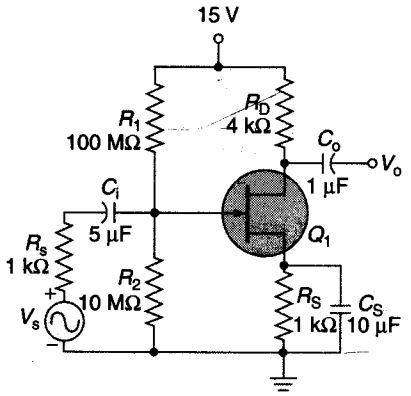


Figure 8.54 | Problem 2.

3. For the single-stage amplifier shown in Figure 8.55, determine the values of

a. $A_{vs} = V_o/V_s$
b. $A_v = V_o/V_i$
c. $A_i = I_o/I_i$

(Given that $h_{fe} = 100$, $h_{ie} = 1$ kΩ and that the effect of h_{oe} can be neglected.)

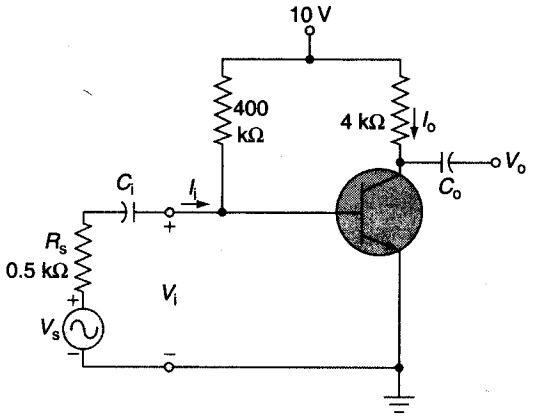


Figure 8.55 | Problem 3.

4. For the BJT configuration shown in Figure 8.56, determine the following:

a. V_i
b. Z_i
c. A_{vnl}
d. A_{vs}

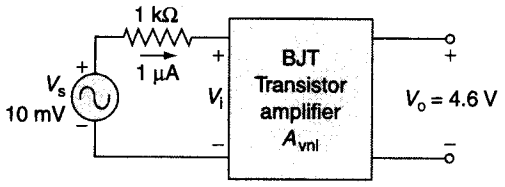


Figure 8.56 | Problem 4.

5. For the amplifier shown in Figure 8.57, determine the following:
   a. DC bias currents and voltages to produce a quiescent output voltage of 7.5 V
   b. Z_i
   c. Z_o
   (Given that the h_{fe}, h_{ie} and h_{oe} parameters of both the transistors are 149, 1 kΩ and 25 × 10^{-4} Ω^{-1}, respectively, $V_{BE1} = V_{BE2} = 0.7$ V and $R_s = 500$ Ω.)

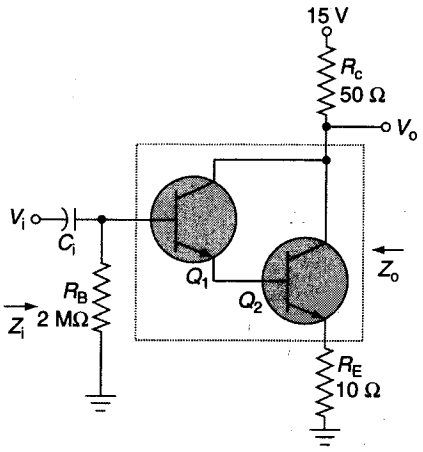


Figure 8.57 | Problem 5.

ANSWERS

Multiple-Choice Questions

1. (a)	**3.** (a)	**5.** (e)	**7.** (c)	**9.** (e)
2. (c)	**4.** (a)	**6.** (d)	**8.** (b)	**10.** (d)

Fill in the Blanks

1. Highest, lowest
2. Coupling, bypass, stray
3. Emitter–follower, infinite
4. Input, input, impedance
5. Norton's equivalent, gate-source voltage (V_{gs})

Problems

1. 1200, 882.12 Ω, 2 kΩ
2. 9.09 MΩ, 3.7 kΩ, −7.41
3. −266.31, −400, 99.75
4. 9 mV, 9 kΩ, 511.11, 460
5. $I_{CQ2} = 150$ mA, $I_{EQ2} = 150$ mA, $I_{BQ2} = 1$ mA, $I_{EQ1} = 1$ mA, $I_{BQ1} = 6.67$ μA, $I_{CQ1} = 1$ mA, $V_{CQ2} = 7.5$ V, $V_{CQ1} = 7.5$ V, $V_{EQ2} = 1.5$ V, $V_{EQ1} = 2.2$ V, $V_{BQ2} = 2.2$ V, $V_{BQ1} = 2.9$ V, $Z_i = 46.51$ kΩ, $Z_o = 6.73$ Ω

CHAPTER 9

High-Frequency Response of Small Signal Amplifiers

Learning Objectives

After completing this chapter, you will learn the following:

- High-frequency model for the common-emitter transistor amplifier configuration.
- Common-emitter short-circuit current gain.
- β cut-off frequency and α cut-off frequency.
- High-frequency response of common-collector transistor amplifier configuration.
- High-frequency response of cascaded amplifier stages.
- High-frequency response of an FET amplifier.
- Amplifier rise time and sag.

The focus in this chapter is on the high-frequency response of small signal amplifiers. The high-frequency response of BJT amplifiers is studied using the hybrid-Π model. High-frequency response of common-emitter, common-collector and common-base BJT amplifiers and FET amplifiers is discussed in the chapter. This is followed by discussion on high-frequency response of cascaded amplifier stages. Other topics discussed in the chapter are Miller's Theorem and amplifier's response to a square input waveform. The chapter is amply illustrated with solved examples.

9.1 High-Frequency Model for the Common-Emitter Transistor Amplifier

The h-parameter model of a transistor is not applicable at high frequencies as at these frequencies the transistor behaves in quite a different manner to what it does at low frequencies. At low frequencies, it is assumed that the transistor responds to the input voltage and current instantly as the diffusion time of the carriers is very small as compared to the rise time of the input signal. However, at high frequencies this is not the case and hence the h-parameter model is not valid at high frequencies. A commonly used model at high frequencies is the hybrid-Π model or the Giacoletto model. This model gives a fairly good approximation of the transistor's behavior at high frequencies.

Figures 9.1(a) and (b) show the circuit of a common-emitter NPN transistor and its hybrid-Π model, respectively. The node B′ is an internal node and is not physically accessible. All the components, both capacitive as well as resistive, are assumed to be independent of frequency. They are dependent on the quiescent operating conditions, but under a given bias condition they do not vary much for small input signal variations.

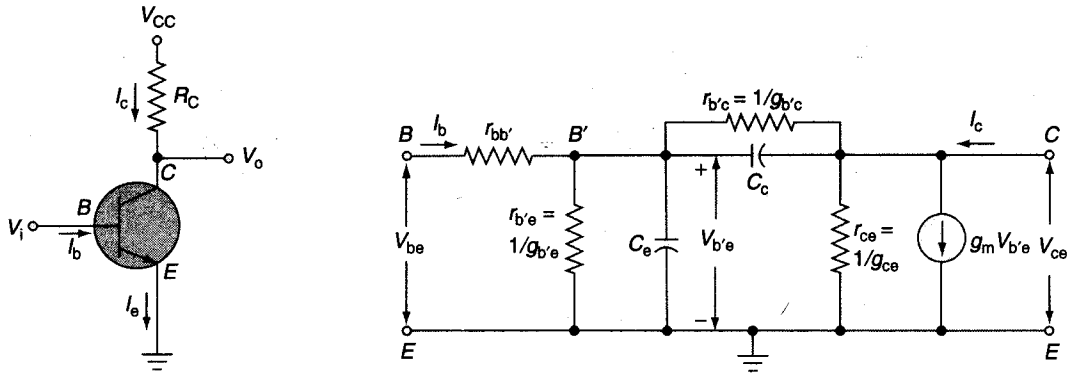


Figure 9.1 (a) Common-emitter NPN transistor; (b) hybrid-Π model of the common-emitter transistor of part (a).

Various circuit components are the base-spreading resistance ($r_{bb'}$), conductance between terminals B′ and E ($g_{b'e}$), conductance between terminals C and E (g_{ce}), conductance between terminals B′ and C ($g_{b'c}$), current source between terminals C and E ($g_m V_{b'e}$), collector-junction barrier capacitance (C_c) and diffusion capacitance between terminals B′ and E (C_e). The ohmic base-spreading resistance ($r_{bb'}$) is represented as a lump parameter between the external base terminal (B) and the node B′. The conductance ($g_{b'e}$) takes into account the increase in the recombination base current due to the increase in the minority carriers in the base region. g_{ce} is the conductance between the collector and the emitter terminals. The conductance ($g_{b'c}$) takes into account the feedback effect between the output and the input due to Early effect. Early effect results in modulation of the width of the base region due to varying collector–emitter voltage which in turn causes a change in the emitter and the collector currents as the slope of the minority-carrier distribution in the base region changes.

Small changes in the value of voltage $V_{b'e}$ cause excess minority carriers, proportional to the voltage $V_{b'e}$, to be injected in to the base region. This results in small signal collector current. Hence, the magnitude of the collector current for shorted collector and emitter terminals is proportional to the voltage $V_{b'e}$. The current generator $g_m V_{b'e}$ takes into account this effect. Note that g_m is the transconductance of the transistor. C_c is the collector-junction barrier capacitance. Sometimes, this capacitance is split into two parts, namely, the capacitance between C and B′ terminals and the capacitance between C and B terminals. The capacitance between C and B terminals is also referred to as the overlap-diode capacitance.

In this section, we will derive the expressions for the components of hybrid-Π model in terms of h-parameters.

Hybrid-Π Conductances

Figure 9.2(a) shows the hybrid-Π model for the common-emitter transistor amplifier applicable at low frequencies and Figure 9.2(b) shows the h-parameter model for the same. As the hybrid-Π model is drawn for low frequencies, the capacitive elements are considered as open circuit.

Base-Spreading Resistance ($r_{bb'}$)

In the circuit shown in Figure 9.2(b), the value of input resistance when the output terminals are shorted, that is $V_{ce} = 0$, is equal to h_{ie}. Under these conditions for the circuit in Figure 9.2(a), the input resistance is given by

$$Z_i\Big|_{V_{ce}=0} = r_{bb'} + r_{b'e} \| r_{b'c} \tag{9.1}$$

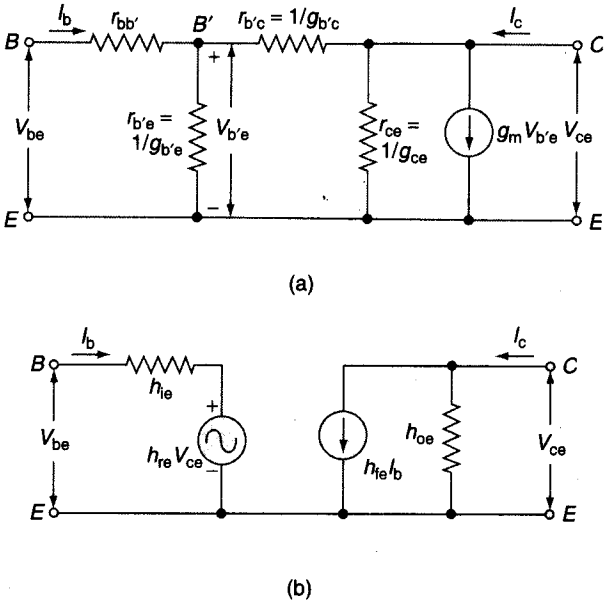


Figure 9.2 (a) Hybrid-Π model for a common-emitter transistor at low frequencies; (b) h-parameter model for a common-emitter transistor at low frequencies.

Therefore

$$h_{ie} = r_{bb'} + r_{b'e} \| r_{b'c} \tag{9.2}$$

As $r_{b'c} >> r_{b'e}$, therefore Eq. (9.2) can be approximated as

$$h_{ie} = r_{bb'} + r_{b'e} \tag{9.3}$$

Conductance between Terminals B' and C or the Feedback Conductance ($g_{b'c}$)

For the circuit in Figure 9.2(b), if the input terminals are open-circuited, then h_{re} is the reverse voltage gain. In terms of the circuit in Figure 9.2(a), the value of h_{re} is given by

$$h_{re} = \frac{V_{b'e}}{V_{ce}} = \frac{r_{b'e}}{r_{b'e} + r_{b'c}} \tag{9.4}$$

Arranging the terms in Eq. (9.4), we get

$$r_{b'e}(1 - h_{re}) = h_{re} r_{b'c} \tag{9.5}$$

As the value of h_{re} is in the range of 10^{-4}, that is, $h_{re} << 1$, therefore Eq. (9.5) can be approximated by

$$r_{b'e} = h_{re} r_{b'c} \text{ or } g_{b'c} = h_{re}\, g_{b'e} \tag{9.6}$$

The equation also verifies that the value of resistance $r_{b'c}$ is much larger than resistance ($r_{b'e}$), that is, $r_{b'c} >> r_{b'e}$.

Conductance between Terminals C and E (g_{ce})

For the circuit in Figure 9.2(b), if the input terminals are open circuit then

$$V_{b'e} = h_{re} V_{ce} \tag{9.7}$$

For the circuit in Figure 9.2(a), with the input terminals open, that is with $I_b = 0$, the collector current I_c is given by

$$I_c = \frac{V_{ce}}{r_{ce}} + \frac{V_{ce}}{r_{b'e} + r_{b'c}} + g_m V_{b'e} \tag{9.8}$$

Value of h_{oe} is given by

$$h_{oe} = \left.\frac{I_c}{V_{ce}}\right|_{I_b = 0} = \frac{1}{r_{ce}} + \frac{1}{r_{b'e} + r_{b'c}} + \frac{g_m V_{b'e}}{V_{ce}} \tag{9.9}$$

Substituting the value of $V_{b'e}$ given in Eq. (9.7) in Eq. (9.9) we get

$$h_{oe} = \frac{1}{r_{ce}} + \frac{1}{r_{b'e} + r_{b'c}} + g_m h_{re} \tag{9.10}$$

Substituting the value of h_{re} as $g_{b'c}/g_{b'e}$, $1/r_{ce}$ as g_{ce}, $1/r_{b'c}$ as $g_{b'c}$ and assuming that $r_{b'c} >> r_{b'e}$, Eq. (9.10) can be rewritten as

$$h_{oe} = g_{ce} + g_{b'c} + g_m \frac{g_{b'c}}{g_{b'e}} \tag{9.11}$$

We will derive latter that the value of g_m is given by

$$g_m = h_{fe}\, g_{b'e} \tag{9.12}$$

Substituting the value of g_m given by Eq. (9.12) in Eq. (9.11), we get

$$h_{oe} = g_{ce} + g_{b'c} + g_{b'c} h_{fe} \tag{9.13}$$

Rearranging the terms in the above equation we get

$$g_{ce} = h_{oe} - (1 + h_{fe}) g_{b'c} \tag{9.14}$$

As the value of $h_{fe} >> 1$, Eq. (9.14) can be approximated as

$$g_{ce} \cong h_{oe} - h_{fe} g_{b'c} \cong h_{oe} - g_m h_{re} \tag{9.15}$$

Conductance between Terminals B' and E or the Input Conductance ($g_{b'e}$)

In the circuit shown in Figure 9.2(a) as the value of resistance ($r_{b'c}$) is much greater than resistance ($r_{b'e}$), most of the current I_b flows into $r_{b'e}$ and the value of the voltage ($V_{b'e}$) is given by

$$V_{b'e} \cong I_b r_{b'e} \tag{9.16}$$

The short-circuit collector current (I_c) is given by

$$I_c = g_m V_{b'e} \cong g_m I_b r_{b'e} \tag{9.17}$$

As we have studied in Chapter 8, the short-circuit current gain (h_{fe}) is defined as

$$h_{fe} = \left.\frac{I_c}{I_b}\right|_{V_{ce} = \text{const.}} = g_m r_{b'e} \tag{9.18}$$

Rearranging the terms in Eq. (9.18), we get

$$r_{b'e} = \frac{h_{fe}}{g_m} \text{ or } g_{b'e} = \frac{g_m}{h_{fe}} \tag{9.19}$$

Transistor's Transconductance (g_m)

The transconductance of a transistor (g_m) is defined as the ratio of the change in the value of collector current to change in the value of voltage $V_{b'e}$ for constant value of collector–emitter voltage.

For a common-emitter transistor configuration, the expression for collector current is given by

$$I_c = I_{CO} + \alpha I_e \tag{9.20}$$

The value of g_m is given by

$$g_m = \left.\frac{\partial I_c}{\partial V_{b'e}}\right|_{V_{CE} = \text{const.}} = \alpha \frac{\partial I_e}{\partial V_{b'e}} = \alpha \frac{\partial I_e}{\partial V_e} \tag{9.21}$$

The partial derivative of the emitter voltage w.r.t. to the emitter current (i.e., $\partial V_e / \partial I_e$) can be represented as the emitter diode resistance (r_e). As we have studied in Chapter 2 on semiconductor diodes, the dynamic resistance of a forward-biased diode (r_d) is given as

$$r_d = \frac{V_T}{I_D} \tag{9.22}$$

where V_T is the volt equivalent of temperature and I_D is the diode current. Therefore, the value of g_m can be generalized as

$$g_m = \frac{\alpha I_e}{V_T} = \frac{I_c - I_{CO}}{V_T} \tag{9.23}$$

As the value of $I_c >> I_{CO}$, therefore the value of g_m for an NPN transistor is positive. For a PNP transistor, the analysis can be carried out on similar lines and the value of g_m in the case of a PNP transistor is also positive. Therefore, the expression for g_m can be written as

$$g_m = \frac{|I_c|}{V_T} \tag{9.24}$$

Hybrid-Π Capacitances

In the hybrid-Π model shown in Figure 9.1(b), there are two capacitances namely the collector-junction barrier capacitance (C_c) and the emitter-junction diffusion capacitance (C_e).

Collector-Junction Capacitance (C_c)

The capacitance C_c is the output capacitance of the common-base transistor configuration with the input open ($I_e = 0$). It is also specified as C_{ob}. As the collector–base junction is reverse-biased, C_c is the transition capacitance and it varies as $(V_{CB})^{-n}$, where n is 1/2 for abrupt junction and 1/3 for a graded junction.

Emitter-Junction Capacitance (C_e)

The capacitance C_e is the diffusion capacitance of the forward-biased emitter junction and is proportional to the emitter current (I_e) and is almost independent of temperature.

Variation of Hybrid-Π Parameters

The variations in the values of hybrid-Π parameters with change in collector current (I_C), collector–emitter voltage (V_{CE}) and temperature (T) are highlighted in Table 9.1.

Table 9.1 | Variations in the values of hybrid-Π parameters

Parameter	$I_C\uparrow$	$V_{CE}\uparrow$	$T\uparrow$
g_m	Linear	Independent	Inverse
$r_{bb'}$	Decreases	Complex relation	Increases
$r_{b'e}$	Inverse	Increases	Increases
C_e	Linear	Decreases	Complex relation
C_c	Independent	Decreases	Increases

9.2 Common-Emitter Short-Circuit Current Gain

Let us consider a single-stage common-emitter amplifier with the value of the collector resistor (R_C) equal to zero. In this case as the collector resistor acts as the load resistor, this means that the load is short circuit. Figure 9.3(a) shows the circuit connection and Figure 9.3(b) shows the hybrid-Π equivalent model for the circuit. The input source is a sinusoidal source and furnishes a sinusoidal input current I_i. The load current produced is I_L. The equivalent model shown in the figure can be simplified to that shown in Figure 9.3(c). The assumptions made in the simplified model are that the conductance $g_{b'c}$ can be neglected as the value of $g_{b'c} << g_{b'e}$. The conductance g_{ce} has also been removed as it is placed across short-circuited terminals. Another approximation is that the current delivered directly to the output through the conductance $g_{b'c}$ and capacitance C_c has been neglected.

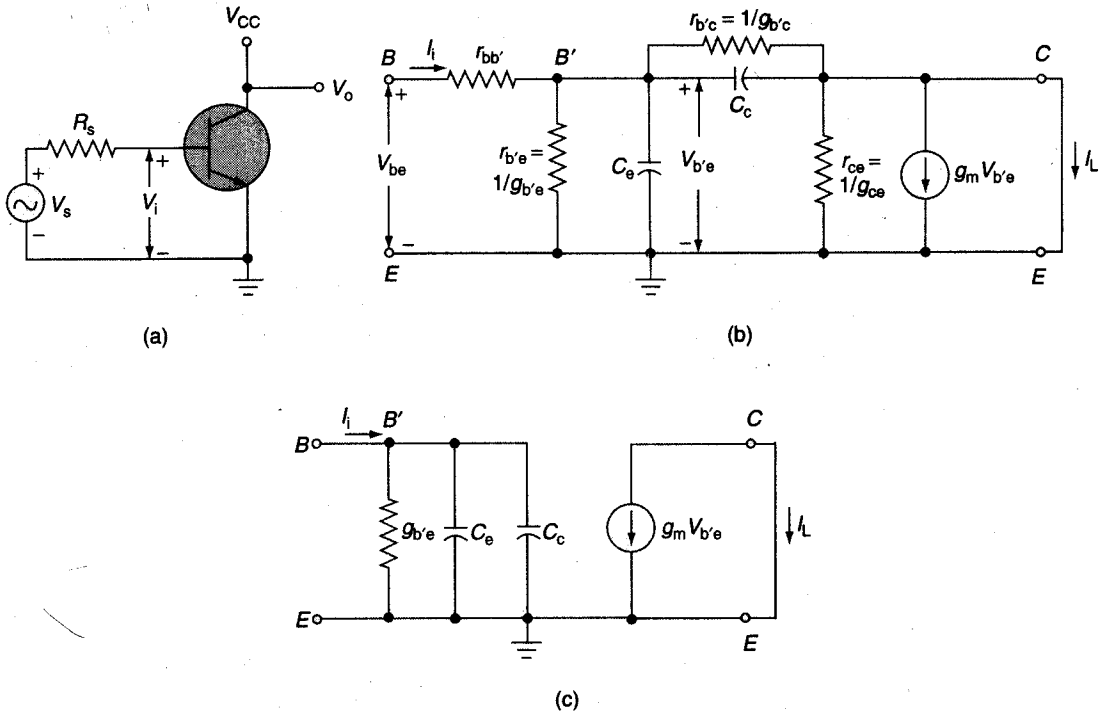


Figure 9.3 | (a) Common-emitter amplifier with short-circuit load; (b) hybrid-Π equivalent model for the amplifier in part (a); (c) simplified hybrid-Π equivalent model.

The parameters of interest are the β cut-off frequency (f_β) and the short-circuit gain bandwidth product (f_T). f_β is the frequency at which the value of short-circuit common-emitter gain reduces to 0.707 times its mid-band value. In other words, at the β cut-off frequency, the short-circuit common-emitter current gain is 3 dB below its mid-band value. Thus, f_β represents the maximum attainable current gain bandwidth for the common-emitter amplifier. The actual maximum bandwidth depends upon the circuit connections. f_T is the frequency at which the short-circuit common-emitter current gain value is unity or 0 dB.

β Cut-Off Frequency

For the circuit shown in Figure 9.3(c), the value of load current (I_L) is given by

$$I_L = -g_m V_{b'e} \tag{9.25}$$

The value of $V_{b'e}$ is given by

$$V_{b'e} = \frac{I_i}{g_{b'e} + j\omega(C_e + C_c)} \tag{9.26}$$

The value of current gain (A_i) under short-circuit condition is

$$A_i = \frac{I_L}{I_i} \tag{9.27}$$

Substituting the values of I_L and I_i given by Eqs. (9.25) and (9.26), respectively, in Eq. (9.27) we get

$$A_i = \frac{-g_m}{g_{b'e} + j\omega(C_e + C_c)} \tag{9.28}$$

Rearranging the terms in Eq. (9.28) we get

$$A_i = \frac{-g_m / g_{b'e}}{1 + [j\omega(C_e + C_c)/g_{b'e}]} \tag{9.29}$$

From Eq. (9.19) we know that

$$g_{b'e} = \frac{g_m}{h_{fe}}$$

Therefore, the value of current gain A_i is given by

$$A_i = \frac{-h_{fe}}{1 + [j\omega(C_e + C_c)/g_{b'e}]} = \frac{-h_{fe}}{1 + [j2\pi f(C_e + C_c)/g_{b'e}]} \tag{9.30}$$

At low frequencies, the value of current gain A_i is given by

$$A_i = -h_{fe} \tag{9.31}$$

f_β is the frequency at which the value of current gain reduces to 0.707 times the gain value given in Eq. (9.31). Therefore,

$$A_i = \frac{-h_{fe}}{1 + j(f/f_\beta)} \tag{9.32}$$

Magnitude of current gain (A_i) is given by

$$|A_i| = \frac{h_{fe}}{\sqrt{1 + (f/f_\beta)^2}}$$

The value of f_β is given by

$$f_\beta = \frac{g_{b'e}}{2\pi(C_e + C_c)} \tag{9.33}$$

As we can see from Eq. (9.31), the value of A_i is equal to $-h_{fe}$ at zero and low frequencies. Remember that h_{fe} is the low-frequency short-circuit current gain of the common-emitter amplifier configuration.

Gain-Bandwidth Product

The frequency f_T is the frequency at which the magnitude of the short-circuit current gain of the common-emitter amplifier configuration becomes unity. As the value of $h_{fe} >> 1$, the magnitude of the current gain A_i becomes unity at the frequency given by the product of h_{fe} and f_β. Therefore, f_T is given by

$$f_T \cong h_{fe} f_\beta \cong \frac{h_{fe} g_{b'e}}{2\pi(C_e + C_c)} \cong \frac{g_m}{2\pi(C_e + C_c)} \tag{9.34}$$

The parameter f_T is a strong function of the collector current of the transistor. The variation of f_T with collector current (I_c) is highlighted in Figure 9.4.

The expression for current gain A_i can be written as

$$A_i \cong \frac{-h_{fe}}{1 + jh_{fe}(f/f_T)} \tag{9.35}$$

Figure 9.5 shows the variation of the current gain of the short-circuit common-emitter amplifier configuration with frequency. The dotted bold lines indicate the asymptotic curves while the regular bold line shows the actual curve. The two asymptotes intersect each other at $f = f_\beta$ and the gain thereafter decreases at a rate of 20 dB/decade. The actual gain at $f = f_\beta$ is 3 dB down (or 0.707 times) the value of mid-band gain.

α Cut-Off Frequency

The α cut-off frequency is the frequency at which the short-circuit current gain value of the common-base configuration drops by 3 dB to its value at low frequencies. It is represented as f_α. It may be mentioned here that the transistor used in common-base configuration has a much higher value of 3 dB frequency as compared to the transistor used in common-emitter configuration. In other words, the value of f_α is much larger than the value of f_β.

The expression for the current gain of the common-base amplifier configuration is given by

$$A_i = \frac{-h_{fb}}{1 + j(f/f_\alpha)} \tag{9.36}$$

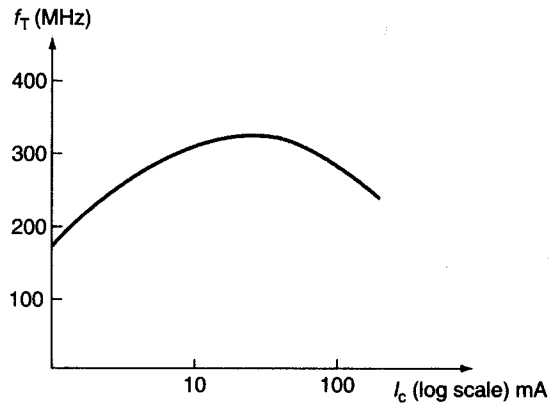


Figure 9.4 | Variation of the frequency f_T with collector current.

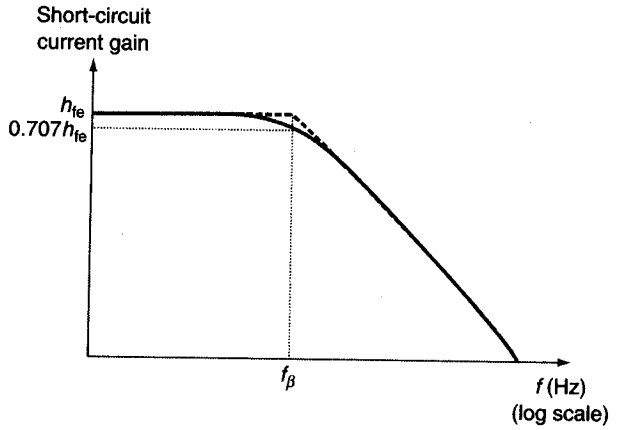


Figure 9.5 | Variation of short-circuit common-emitter current gain with frequency.

where f_α is the α cut-off frequency. The expression for the α cut-off frequency is given by

$$f_\alpha = \frac{1}{2\pi r_{b'e}(1+h_{fb})C_e} \tag{9.37}$$

As the value of $h_{fe} \cong 1/(1 + h_{fb})$, Eq. (9.37) can be rewritten as

$$f_\alpha \cong \frac{h_{fe}}{2\pi r_{b'e}C_e} \tag{9.38}$$

Multiplying and dividing Eq. (9.38) by $(C_e + C_c)$ and substituting the value of f_β in the equation, we get

$$f_\alpha \cong \frac{h_{fe}f_\beta(C_e+C_c)}{C_e} \tag{9.39}$$

From the above equation, it is clear that the bandwidth offered by the common-base amplifier is much higher than that offered by the common-emitter amplifier, although the latter has much higher value of gain. Figure 9.6 shows the comparison of the manner in which short-circuit current gains for the common-emitter and common-base amplifier configurations vary with frequency.

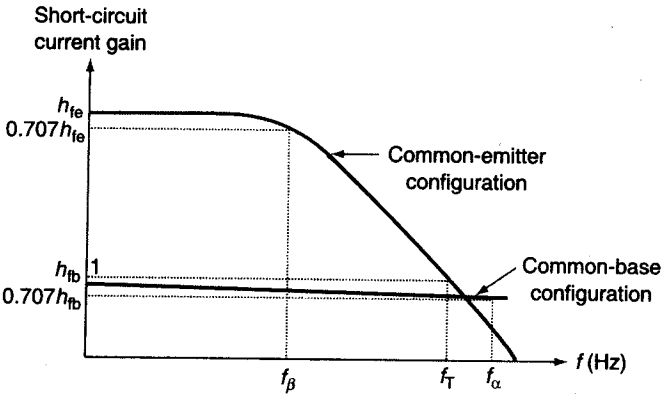


Figure 9.6 | Comparison of variations of short-circuit current gains of common-emitter and common-base amplifier configurations with frequency.

EXAMPLE 9.1 *Determine the α and β cut-off frequencies for a transistor with the following specifications: $g_m = 38$ mmhos, $r_{b'e} = 5.9\ k\Omega$, $h_{ie} = 6\ k\Omega$, $r_{bb'} = 100\ \Omega$, $C_c = 12$ pF, $C_e = 63$ pF, $f_T = 80$ MHz and $h_{fe} = 224$ at 1 kHz. Also determine the value of common-emitter short-circuit current gain at frequencies of f_β, f_T and f_α.*

Solution

1. $f_\alpha = \dfrac{h_{fe}}{2\pi r_{b'e} C_e}$

$$= \frac{224}{2 \times \pi \times 5.9 \times 10^3 \times 63 \times 10^{-12}} = 95.91 \text{ MHz}$$

2. $f_\beta = \dfrac{g_{b'e}}{2\pi(C_e + C_c)}$

3. $g_{b'e} = 1/r_{b'e} = 1/(5.9 \times 10^3) = 1.69 \times 10^{-4}$.

4. $f_\beta = 1.69 \times 10^{-4}/[2 \times \pi \times (63 \times 10^{-12} + 12 \times 10^{-12})] = 358.63$ kHz.

5. Common-emitter short-circuit current gain is given by

$$A_i = \frac{-h_{fe}}{1 + j(f/f_\beta)}$$

6. For $f = f_\alpha$, $A_i = -224/[1 + j\{(95.91 \times 10^6)/(358.63 \times 10^3)\}] = -224/(1 + 267.43j)$.

7. $|A_i| = 224/\sqrt{(1^2 + 267.43^2)} = 0.838$.

8. $\angle A_i = 90° - \tan^{-1}(267.43) = 90° - 89.786° = 0.21°$.

9. For $f = f_\beta$, $A_i = -224/[1 + j\{(358.63 \times 10^3)/(358.63 \times 10^3)\}] = -224/(1 + j)$.

10. $|A_i| = 224/\sqrt{2} = 158.39$.

11. $\angle A_i = 90° - \tan^{-1}1 = 90° - 45° = 45°$.

12. $f_T = h_{fe} f_\beta$.

13. $f_T = 224 \times 358.63 \times 10^3 = 80.333$ MHz.

14. For $f = f_T$, $A_i = -224/[1 + j\{(80.333 \times 10^6)/(358.63 \times 10^3)\}] = -224/(1 + 224j)$.

15. $|A_i| = 224/\sqrt{(1^2 + 224^2)} = 1$.

16. $\angle A_i = 90° - \tan^{-1}224 = 90° - 89.744° = 0.256°$.

9.3 Miller's Theorem

Let us consider a circuit configuration shown in Figure 9.7(a). As shown in the figure, it comprises three nodes, namely, input node 1, output node 2 and a ground node G. An impedance (Z) is connected between the input and the output nodes. This impedance is also referred to as the feedback impedance. This impedance has an effect on the functioning of the circuit. It is very difficult to analyze such a network as the impedance affects the input and the output simultaneously. Miller's theorem helps to analyze such circuit configurations. According to Miller's theorem, the circuit with feedback impedance can be replaced by an equivalent circuit such that the

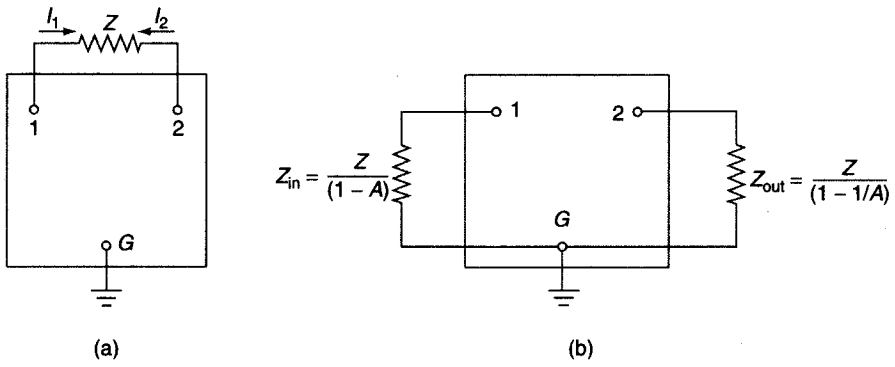


Figure 9.7 (a) Circuit configuration with feedback impedance; (b) Miller's equivalent circuit of the network in part (a).

feedback impedance is split into two impedances: one between the input terminal and ground (Z_{in}) and the other between the output terminal and ground (Z_{out}). Figure 9.7(b) shows the Miller's equivalent circuit of the network shown in Figure 9.7(a). In the subsequent paragraphs, we derive the expressions for Z_{in} and Z_{out}.

Let the voltages at nodes 1 and 2 be V_1 and V_2, respectively. Let the ratio of V_2/V_1 be represented as A. Using Miller's theorem, the impedance connected between nodes 1 and 2 can be replaced by two impedances: one between node 1 and ground node G (Z_{in}) and the other between node 2 and ground node G (Z_{out}). The value of current I_1 is given by

$$I_1 = \frac{V_1 - V_2}{Z} \tag{9.40}$$

The value of V_2 is given by

$$V_2 = AV_1$$

Therefore, current I_1 is given as

$$I_1 = \frac{V_1 - AV_1}{Z} = \frac{V_1(1-A)}{Z} \tag{9.41}$$

From Eq. (9.41), the ratio of V_1/I_1 is given by

$$\frac{V_1}{I_1} = \frac{Z}{1-A} \tag{9.42}$$

V_1/I_1 is the equivalent impedance of Z as seen from the input side of the circuit. Therefore, Z_{in} is equal to the ratio V_1/I_1 and is given by

$$Z_{in} = \frac{Z}{1-A} \tag{9.43}$$

The impedance Z_{in} appears in parallel with the input terminals of the network. The expression for output impedance Z_{out} can be derived as follows. The value of current I_2 is given by

$$I_2 = \frac{V_2 - V_1}{Z} \tag{9.44}$$

Voltage V_1 is expressed in terms of voltage V_2 as

$$V_1 = \frac{V_2}{A}$$

Substituting this value of V_1 in Eq. (9.44) we get

$$I_2 = \frac{V_2 - (V_2/A)}{Z} = \frac{V_2[1-(1/A)]}{Z} \tag{9.45}$$

The ratio V_2/I_2 is given by

$$\frac{V_2}{I_2} = \frac{Z}{[1-(1/A)]} \tag{9.46}$$

The ratio V_2/I_2 is the equivalent impedance of Z as seen from the output terminals. It is therefore equal to Z_{out}. The expression for Z_{out} is given by

$$Z_{out} = \frac{Z}{1-(1/A)} \tag{9.47}$$

EXAMPLE 9.2 *For the circuit shown in Figure 9.8, determine the values of following parameters: (a) R_i; (b) R_i'; (c) amplifier voltage gain (A_v); (d) system voltage gain (A_{vs}); (e) amplifier current gain (A_i) and (f) system current gain (A_i'). The value of transistor's h-parameters are $h_{ie} = 1\ k\Omega$, $h_{re} = 1 \times 10^{-4}$, $h_{fe} = 100$ and $h_{oe} = 25 \times 10^{-6}\ \Omega^{-1}$.*

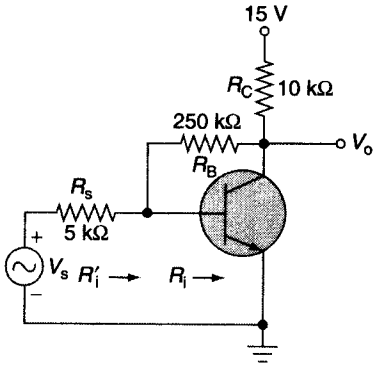


Figure 9.8 | Example 9.1.

Solution

1. The resistor R_B is the feedback resistor between the input and the output terminals. It can be replaced by the Miller's equivalent components as shown in Figure 9.9. The equivalent impedance of R_B as seen from the output terminals (R_{BO}) is given by $R_B/[1-(1/A_v)]$. A_v is the voltage gain from base to collector. As the value of voltage gain is much larger than 1, therefore, value of $R_{BO} \cong R_B \cong 250\ k\Omega$.
2. The effective load resistance $(R_L') = R_C \parallel R_{BO} = 10 \times 10^3 \parallel 250 \times 10^3 = 9.61 \times 10^3\ \Omega = 9.61\ k\Omega$.
3. The value of input resistance R_i is given by

$$R_i = h_{ie} - \frac{h_{re}h_{fe}R_L'}{1+h_{oe}R_L'}$$

$$= 1\times10^3 - \frac{1\times10^{-4}\times100\times9.61\times10^3}{1+25\times10^{-6}\times9.61\times10^3}$$

$$= 1000 - \frac{96.1}{1.24} = 1000 - 77.5 = 922.5\ \Omega$$

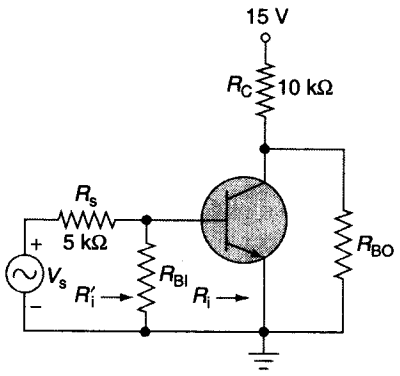


Figure 9.9 | Solution to Example 9.2.

4. Current gain is given by

$$A_i = -\frac{h_{fe}}{1 + h_{oe} R_L'}$$

$$= \frac{-100}{1 + 25 \times 10^{-6} \times 9.61 \times 10^3} = -80.63$$

5. The value of voltage gain is given by

$$A_v = \frac{A_i R_L'}{R_i}$$

$$= \frac{-80.63 \times 9.61 \times 10^3}{922.5} = -839.95$$

6. The value of the effective resistance of R_B from the input side $(R_{BI}) = R_B/[1 - A_v]$ $= 250 \times 10^3 / [1 - (-839.95)] = (250 \times 10^3)/840.95 = 297.28\ \Omega$.

7. The value of $R_i' = R_i \parallel R_{BI} = 922.5 \parallel 297.28 = 224.83\ \Omega$.

8. System voltage gain A_{vs} is given by

$$A_{vs} = A_v \times [R_i'/(R_i' + R_s)]$$

$$= -839.95 \times [224.83/(224.83 + 5 \times 10^3)]$$

$$= -839.95 \times 0.043 = -36.12$$

9. The value of system current gain A_i' is given by

$$A_i' = A_i \times \left(\frac{R_{RI}}{R_i + R_{BI}}\right) \times \left(\frac{R_{BO}}{R_{BO} + R_C}\right)$$

$$= -80.63 \times \frac{297.28}{922.5 + 297.28} \times \frac{250 \times 10^3}{250 \times 10^3 + 10 \times 10^3}$$

$$= -80.63 \times \frac{297.28}{1219.78} \times \frac{250}{260}$$

$$= -80.63 \times 0.244 \times 0.96 = -18.89$$

9.4 Common-Emitter Current Gain with Resistive Load

Figure 9.10(a) shows the circuit diagram of the common-emitter amplifier configuration when the load resistor (R_L) is not equal to zero and Figure 9.10(b) shows its hybrid-Π equivalent model. The conductance $g_{b'c}$ can be replaced by its Miller's equivalent components. The conductance component due to $g_{b'c}$ on the input side is given by $g_{b'c}(1 - K)$, where $K = V_{ce}/V_{b'e}$. The value of K is equal to $-g_m R_L$. The conductance component due to $g_{b'c}$ on the output side is given by $g_{b'c}[(K-1)/K]$. The Miller's component of the capacitance C_c on the input side is given by $C_c(1 - K)$ and on the output side is given by $C_c[(K-1)/K]$. Figure 9.11 shows the equivalent circuit with components $g_{b'c}$ and C_c being replaced by their Miller's equivalent components.

The circuit has two time constants, one associated with the input section and the other associated with the output section. As the value of $K >> 1$, therefore the value of $[(K-1)/K] \cong 1$. Therefore, $g_{b'c}[(K-1)/K] \cong g_{b'c}$ and $C_c[(K-1)/K] \cong C_c$. The total load resistance R_L' is given by

$$R_L' = R_L \| (1/g_{b'c}) \| (1/g_{ce}) \tag{9.48}$$

In most cases, the value of $g_{b'c} << g_{ce}$ ($r_{b'c} \approx 4$–5 MΩ and $r_{ce} \approx 80$–100 kΩ), therefore $g_{b'c}$ can be ignored from the output section. The value of load resistor R_L is in the range of 2–5 kΩ. Therefore, the conductance g_{ce} can be neglected as compared to $1/R_L$. Therefore, resistor $R_L' \cong R_L$.

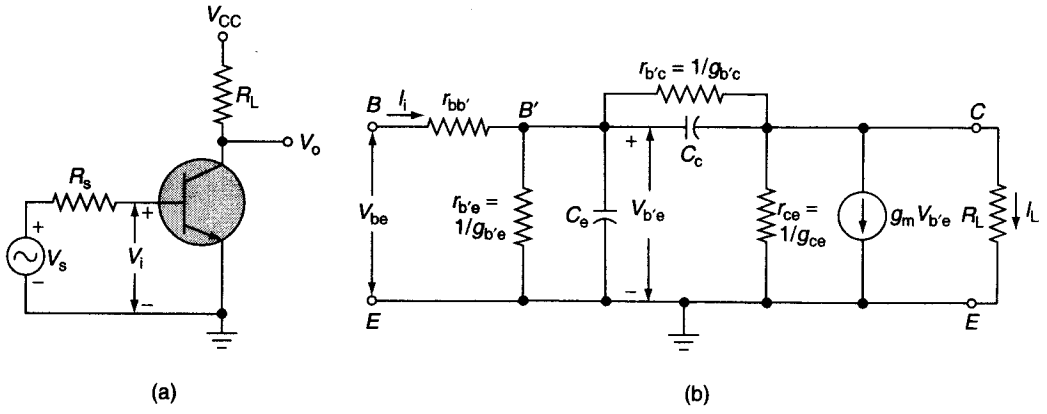


Figure 9.10 | (a) Circuit diagram of common-emitter amplifier configuration with load resistance (R_L); (b) hybrid-Π equivalent model of the circuit in part (a).

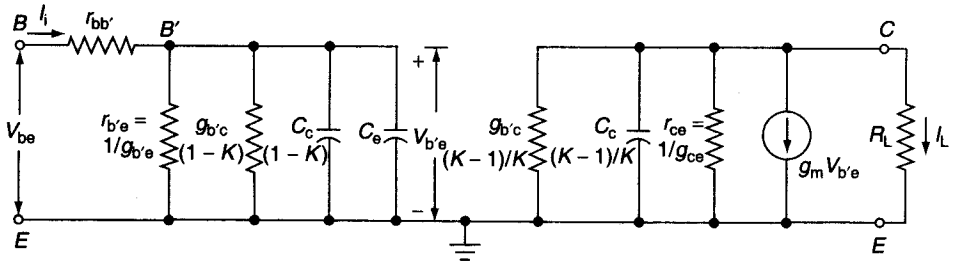


Figure 9.11 | Simplified hybrid-Π model making use of Miller's theorem for the model shown in Figure 9.10(b).

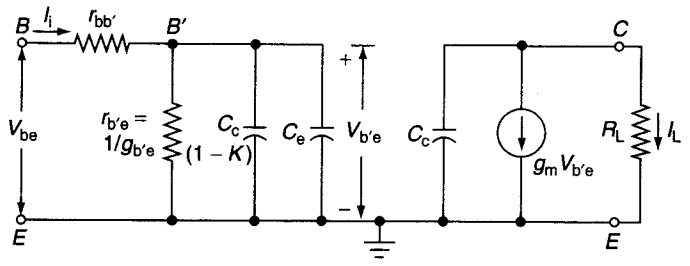


Figure 9.12 | Further simplified hybrid-Π model for the model shown in Figure 9.10(b).

The input conductance (g_i) is given by

$$g_i = g_{b'e} + g_{b'c}(1-K) \tag{9.49}$$

In most of the cases, the magnitude of the conductance $g_{b'c}(1-K)$ is very small as compared to the value of $g_{b'e}$. Therefore, $g_i \cong g_{b'e}$. Figure 9.12 shows the further simplified hybrid-Π equivalent model.
The output time constant (t_{oc}) is given by

$$t_{oc} = R_L' C_c \approx R_L C_c \tag{9.50}$$

The input time constant (t_{ic}) is given by

$$t_{ic} = (1/g_i) \times [C_e + C_c(1 + g_m R_L) \approx (1/g_{b'e})] \times [C_e + C_c(1 + g_m R_L)] \tag{9.51}$$

In practical situations, the output time constant is negligible as compared to the input time constant and hence can be ignored. It may be mentioned here that if the transistor works into a highly capacitive load, then the output time constant will also be predominant and cannot be ignored.

The upper 3 dB frequency in this case is given by

$$f_H = \frac{1}{2\pi r_{b'e}[C_e + C_c(1 + g_m R_L)]} \tag{9.52}$$

The above equation has been derived by neglecting the effect of the base-spreading resistance ($r_{bb'}$) and source resistor (R_s). The value of source resistor has a very strong influence on the upper cut-off frequency. The cut-off frequency taking into account the effect of R_s and $r_{bb'}$ is given by

$$f_H = \frac{1}{2\pi[(R_s + r_{bb'}) \| r_{b'e}][C_e + C_c(1 + g_m R_L)]} \tag{9.53}$$

When the effect of biasing resistors is taken into account, the term R_s in Eq. (9.53) is replaced by $R_{s'}$, where $R_{s'}$ is a parallel combination of R_s and biasing resistors.

9.5 High-Frequency Response of Common-Collector Transistor Amplifier

In this section, we discuss the high-frequency response of a common-collector transistor amplifier. Figure 9.13(a) shows the common-collector transistor amplifier configuration. Capacitance C_L is included in parallel with the load resistor R_L as the common-collector transistor due to its low output resistance is often used to drive capacitive loads. Figure 9.13(b) shows the hybrid-Π equivalent model for the common-collector amplifier configuration shown in Figure 9.13(a).

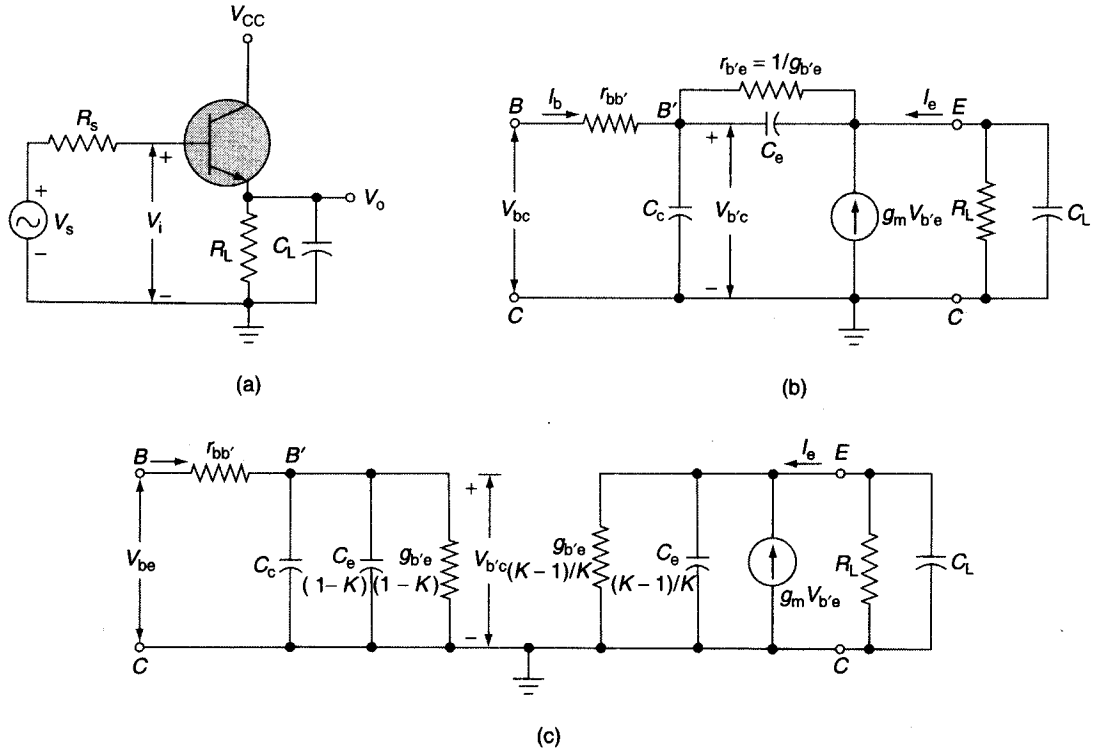


Figure 9.13 (a) Common-collector amplifier; (b) hybrid-Π equivalent model of the common-collector amplifier; (c) simplified hybrid-Π equivalent model of the common-collector amplifier.

Applying Miller's theorem to the hybrid-Π equivalent circuit of Figure 9.13(b), we get the equivalent circuit as shown in Figure 9.13(c). The parameter K is given by the ratio of voltages V_{ec} and $V_{b'c}$ (i.e., $K = V_{ec}/V_{b'c}$). The input time constant t_{ic} is given by

$$t_{ic} = \left[(R_s + r_{bb'}) \left\| \left\{ \frac{1}{g_{b'e}(1-K)} \right\} \right. \right] [C_c + C_e(1-K)] \tag{9.54}$$

As the low-frequency gain of the emitter–follower configuration is approximately equal to unity, therefore $(1 - K) \cong 0$. Therefore, the expression for t_{ic} can be approximated by

$$t_{ic} \cong (R_s + r_{bb'})C_c \tag{9.55}$$

The output time constant (t_{oc}) is given by

$$t_{oc} = \left[R_L \left\| \left\{ \frac{1}{g_{b'e}(K-1)/K} \right\} \right. \right] [C_L + C_e(K-1)/K] \tag{9.56}$$

As the value of $(K - 1) \cong 0$, the above equation can be simplified as

$$t_{oc} \cong R_L C_L \tag{9.57}$$

As we have assumed that the output load is highly capacitive, therefore the value of $C_L >> C_c$. Hence,

$$R_L C_L >> (R_s + r_{bb'})C_c \tag{9.58}$$

This implies that the value of output time constant (t_{oc}) is much larger than the input time constant (t_{ic}). Hence the upper 3 dB frequency is determined mostly by the output circuit.
The impedance of the output circuit (Z_o) is given by

$$Z_o = R_L \left\| \frac{1}{g_{b'e}(K-1)/K} \right\| \frac{1}{j\omega\{C_L + C_e(K-1)/K\}} \tag{9.59}$$

Substituting $(K-1) \cong 0$, we get

$$Z_o \cong R_L \left\| \frac{1}{j\omega C_L} \right. \tag{9.60}$$

The value of voltage V_{ec} is given by

$$V_{ec} = g_m V_{b'e} Z_o \cong g_m V_{b'e} \left(R_L \left\| \frac{1}{j\omega C_L} \right. \right) \tag{9.61}$$

Rearranging the terms we get

$$V_{ec} = \frac{g_m V_{b'e}}{(1/R_L) + j\omega C_L} = \frac{g_m V_{b'e} R_L}{1 + j\omega R_L C_L} \tag{9.62}$$

The value of $V_{b'e}$ is given by $V_{b'e} = V_{b'c} - V_{ec}$. Therefore, Eq. (9.62) can be rewritten as

$$V_{ec} = \frac{g_m (V_{b'c} - V_{ec}) R_L}{1 + j\omega R_L C_L}$$

The value of V_{ec} is given by

$$V_{ec} = \frac{g_m R_L V_{b'c}}{1 + g_m R_L + j\omega R_L C_L} \tag{9.63}$$

As $K = V_{ec}/V_{b'c}$, therefore the expression for K is given by

$$K = \frac{V_{ec}}{V_{b'c}} = \frac{g_m R_L}{1 + g_m R_L + j\omega R_L C_L} \tag{9.64}$$

Multiplying and dividing Eq. (9.64) by $(1 + g_m R_L)$ we get

$$A = \left(\frac{g_m R_L}{1 + g_m R_L} \right) \frac{1}{1 + [j\omega R_L C_L/(1 + g_m R_L)]} \tag{9.65}$$

Equation (9.65) can be rewritten as Eq. (9.66)

$$A = \left(\frac{g_m R_L}{1 + g_m R_L} \right) \left(\frac{1}{1 + (jf/f_H)} \right) \tag{9.66}$$

where $f_H = (1 + g_m R_L)/2\pi C_L R_L$. The value of f_H can be expressed as

$$f_H = \frac{1 + g_m R_L}{2\pi R_L C_L} \cong \frac{g_m}{2\pi C_L} \tag{9.67}$$

From Eq. (9.34), the value of unity gain bandwidth (f_T) is given by

$$f_T = \frac{g_m}{2\pi(C_e + C_c)} \tag{9.68}$$

As the value of C_e for a transistor is much larger than C_c, therefore f_T can be approximated by

$$f_T \cong \frac{g_m}{2\pi C_e} \tag{9.69}$$

Substituting this value of f_T in Eq. (9.67) we get

$$f_H \cong \frac{f_T C_e}{C_L} \tag{9.70}$$

Since the input impedance between terminals B′ and C is much larger as compared to $(R_s + r_{bb'})$, therefore K is approximately the overall voltage gain (A_{vs}), that is,

$$K \cong A_{vs} = \frac{V_{ec}}{V_s} \tag{9.71}$$

9.6 High-Frequency Response of an FET Amplifier

The high-frequency response of an FET amplifier is similar to that of a BJT amplifier. Figure 9.14 shows the high-frequency model for an FET (JFET as well as MOSFET). The high-frequency model is similar to the low-frequency model with the addition of junction capacitances.

The capacitance C_{gs} represents the barrier capacitance between the gate and the source terminals. C_{gd} is the barrier capacitance between the gate and the drain terminals. C_{ds} is the drain-to-source capacitance of the channel. These capacitors offer high impedance at lower frequencies and can be considered as open circuit. However, at high frequencies, due to these capacitances feedback exists between the input and output circuits and voltage amplification drops rapidly as the frequency increases.

In this section, we discuss the high-frequency response of the common-source and common-drain FET amplifiers. The derivations are done for JFET-based amplifiers. The expressions derived here apply equally well to MOSFET-based amplifiers as well.

Common-Source Amplifier at High Frequencies

Figure 9.15(a) shows the circuit diagram for the common-source JFET amplifier and Figure 9.15(b) shows its small signal high-frequency equivalent model. The output voltage V_o is given by the product of short-circuit current (I) and the impedance seen between the output terminals (Z). Therefore,

$$V_o = ZI \tag{9.72}$$

Z is determined by shorting the input terminals, that is, $V_s = 0$. Hence, there is no current flowing through the current generator $g_m V_s$. Therefore, the value of Z is given by the parallel combination of R_L, $j\omega C_{ds}$, r_d and $j\omega C_{gd}$ and is given by

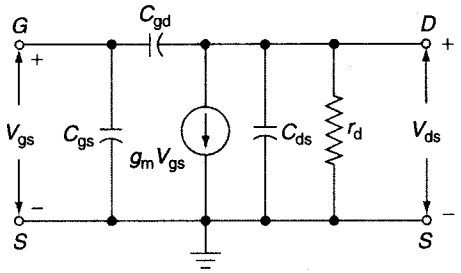


Figure 9.14 | High-frequency model of an FET.

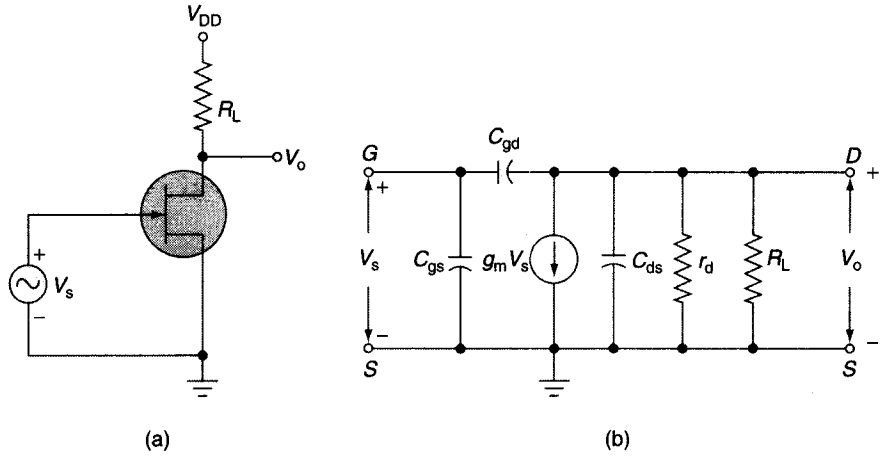


Figure 9.15 (a) Circuit diagram of a common-source JFET amplifier; (b) small signal high-frequency model of the common-source JFET amplifier of part (a).

$$Y = \frac{1}{Z} = G_L + Y_{ds} + g_d + Y_{gd} \tag{9.73}$$

where $G_L = 1/R_L$ is the conductance corresponding to load R_L. If the load is represented by an impedance Z_L, then G_L will be replaced by Y_L (Y_L is the admittance corresponding to impedance Z_L). Also $Y_{ds} = j\omega C_{ds}$ is the admittance corresponding to C_{ds}; $g_d = 1/r_d$ is the conductance corresponding to r_d; $Y_{gd} = j\omega C_{gd}$ is the admittance corresponding to C_{gd}.

The current I flowing from the drain to the source terminal with output terminals shorted is given by

$$I = -g_m V_s + V_s Y_{gd} \tag{9.74}$$

Therefore, the output voltage V_o is given by

$$V_o = \frac{(-g_m + Y_{gd})V_s}{G_L + Y_{ds} + g_d + Y_{gd}} \tag{9.75}$$

The value of voltage gain (A_v) is therefore equal to

$$A_v = \frac{V_o}{V_s} = \frac{-g_m + Y_{gd}}{G_L + Y_{ds} + g_d + Y_{gd}} \tag{9.76}$$

At low frequencies, the FET capacitances can be neglected and hence $Y_{ds} = Y_{gd} = 0$. Therefore, the value of gain at low frequencies is given by

$$A_v = \frac{-g_m}{G_L + g_d} = \frac{-g_m R_L r_d}{R_L + r_d} = -g_m R_L' \tag{9.77}$$

where $R_L' = R_L \| r_d$.

The input admittance and the input capacitance can be calculated as follows. We can see from Figure 9.15(b) that there is a coupling between the gate and the drain terminals through capacitance C_{gd}. The admittance offered by the capacitance (Y_{gd}) can be replaced by $Y_{gd}(1 - A_v)$ between the gate and the source terminals and by $Y_{gd}[1 - (1/A_v)]$ between the drain and the source terminals. The input admittance (Y_i) is therefore given by

$$Y_i = Y_{gs} + (1 - A_v)Y_{gd} = Y_{gs} + (1 + g_m R_L')Y_{gd} \tag{9.78}$$

The input capacitance (C_i) is given by

$$C_i = C_{gs} + (1 - A_v)C_{gd} = C_{gs} + (1 + g_m R_L')C_{gd} \tag{9.79}$$

This input capacitance is important in the case of cascaded amplifiers where the input impedance of a stage acts in shunt across the output impedance of the preceding stage. As the reactance of a capacitance decreases with increase in frequency, the input impedance also decreases and hence the gain of the cascaded amplifier also decreases with increase in frequency.

The output impedance is obtained by the impedance looking into the drain and the source terminals, with the input voltage (V_i) set equal to zero. With $V_i = 0$, the resistance r_d and capacitances C_{ds} and C_{gd} are in parallel. Therefore, the output admittance (Y_o) is given by

$$Y_o = g_d + Y_{ds} + Y_{gd} \tag{9.80}$$

EXAMPLE 9.3 *Calculate the voltage gain of the common-source MOSFET amplifier at operating frequencies of 20 kHz and 20 MHz with drain resistance (R_D) of 100 kΩ. The MOSFET parameters are g_m = 1.5 mA/V, R_D = 50 kΩ, C_{gs} = 2.5 pF, C_{ds} = 1.0 pF and C_{gd} = 2.8 pF.*

Solution

For operating frequency of 20 kHz

1. $Y_{gs} = j\omega C_{gs} = j \times 2 \times \pi \times 20 \times 10^3 \times 2.5 \times 10^{-12} = j3.14 \times 10^{-7}\ \Omega^{-1}$.
2. $Y_{ds} = j\omega C_{ds} = j \times 2 \times \pi \times 20 \times 10^3 \times 1.0 \times 10^{-12} = j1.26 \times 10^{-7}\ \Omega^{-1}$.
3. $Y_{gd} = j\omega C_{gd} = j \times 2 \times \pi \times 20 \times 10^3 \times 2.8 \times 10^{-12} = j3.52 \times 10^{-7}\ \Omega^{-1}$.
4. $g_d = 1/r_d = 1/(50 \times 10^3) = 2 \times 10^{-5}\ \Omega^{-1}$.
5. $G_D = 1/R_D = 1/(100 \times 10^3) = 1 \times 10^{-5}\ \Omega^{-1}$.
6. The value of voltage gain (A_v) is given by

$$A_v = \frac{-g_m + Y_{gd}}{G_D + Y_{ds} + g_d + Y_{gd}}$$

$$= \frac{-1.5\times10^{-3} + j3.52\times10^{-7}}{1\times10^{-5} + j1.26\times10^{-7} + 2\times10^{-5} + j3.52\times10^{-7}}$$

$$= \frac{-1.5\times10^{-3} + j3.52\times10^{-7}}{3\times10^{-5} + j4.78\times10^{-7}}$$

7. The imaginary terms are negligible in comparison with the real terms. Therefore, the value of voltage gain $A_v = (-1.5 \times 10^{-3})/(3 \times 10^{-5}) = -50$.

For operating frequency of 20 MHz

1. $Y_{gs} = j\omega C_{gs} = j \times 2 \times \pi \times 20 \times 10^6 \times 2.5 \times 10^{-12} = j3.14 \times 10^{-4}\ \Omega^{-1}$.
2. $Y_{ds} = j\omega C_{ds} = j \times 2 \times \pi \times 20 \times 10^6 \times 1.0 \times 10^{-12} = j1.26 \times 10^{-4}\ \Omega^{-1}$.
3. $Y_{gd} = j\omega C_{gd} = j \times 2 \times \pi \times 20 \times 10^6 \times 2.8 \times 10^{-12} = j3.52 \times 10^{-4}\ \Omega^{-1}$.

4. $g_d = 1/r_d = 1/(50 \times 10^3) = 2 \times 10^{-5}\ \Omega^{-1}$.
5. $G_D = 1/R_D = 1/(100 \times 10^3) = 1 \times 10^{-5}\ \Omega^{-1}$.
6. The value of voltage gain (A_v) is given by

$$A_v = \frac{-g_m + Y_{gd}}{G_D + Y_{ds} + g_d + Y_{gd}}$$

$$= \frac{-1.5\times10^{-3} + j3.52\times10^{-4}}{1\times10^{-5} + j1.26\times10^{-4} + 2\times10^{-5} + j3.52\times10^{-4}}$$

$$= \frac{-1.5\times10^{-3} + j3.52\times10^{-4}}{3\times10^{-5} + j4.78\times10^{-4}}$$

7. Multiplying and dividing by $(3 \times 10^{-5} - j4.78 \times 10^{-4})$, we get

$$A_v = \frac{(-1.5\times10^{-3} + j3.52\times10^{-4})\times(3\times10^{-5} - j4.78\times10^{-4})}{(3\times10^{-5} + j4.78\times10^{-4})\times(3\times10^{-5} - j4.78\times10^{-4})}$$

$$= \frac{-4.5\times10^{-8} + j7.17\times10^{-7} + j10.56\times10^{-9} + 16.83\times10^{-8}}{9\times10^{-10} + 22.85\times10^{-8}}$$

$$= \frac{-12.33\times10^{-8} + j7.28\times10^{-7}}{22.94\times10^{-8}}$$

8. $|A_v| = \sqrt{[(12.33 \times 10^{-8})^2 + (7.28 \times 10^{-7})^2]}/(22.94 \times 10^{-8}) = 3.22$.
9. $\angle A_v = \tan^{-1}[(7.28 \times 10^{-7})/(-12.33 \times 10^{-8})] = \tan^{-1}(-5.9) = -80.38°$.

Common-Drain Amplifier at High Frequencies

Figure 9.16(a) shows the circuit of a common-drain or a source-follower amplifier. Figure 9.16(b) shows its small signal high-frequency equivalent model.

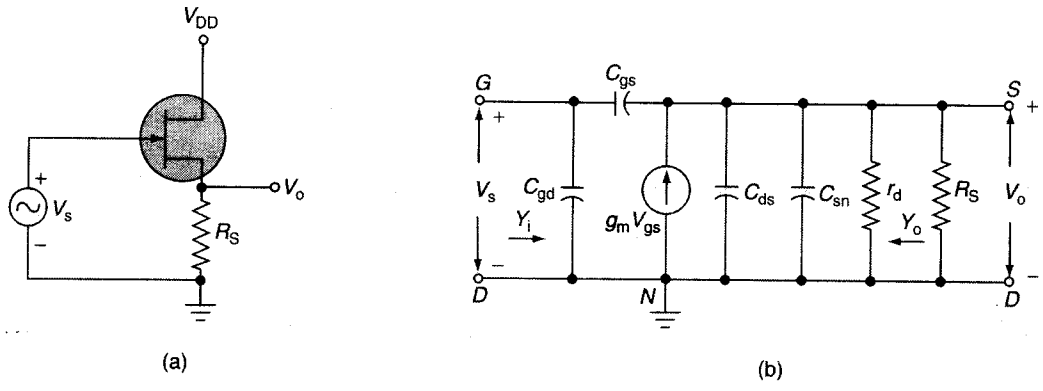


Figure 9.16 (a) Common-drain JFET amplifier; (b) small signal high-frequency equivalent model of the common-drain JFET amplifier shown in part (a).

The output voltage V_o is given by the product of the short-circuit current and the impedance between the source and the ground terminals. By carrying out analysis in a manner similar to that for the common-source amplifier, the expression for the voltage gain (A_v) for a common-drain amplifier is given by

$$A_v = \frac{(g_m + j\omega C_{gs})R_s}{1+[g_m + g_d + j\omega(C_{gs} + C_{ds} + C_{sn})]R_s} \tag{9.81}$$

At low frequencies, the value of reactance offered by the capacitances C_{gs}, C_{ds} and C_{sn} is infinity. Therefore, at low frequencies, the value of voltage gain (A_v) is given by

$$A_v = \frac{g_m R_s}{1+(g_m + g_d)R_s} \tag{9.82}$$

As we can see from the above equation, the value of A_v is slightly less than unity as generally $g_m R_s >> 1$.

Input admittance (Y_i) is obtained by using the Miller's theorem in a manner similar to that done for the common-source FET amplifier. The expression for (Y_i) is given by

$$Y_i = Y_{gd} + Y_{gs}(1 - A_v) = j\omega C_{gd} + j\omega C_{gs}(1 - A_v) \cong j\omega C_{gd} \tag{9.83}$$

One of the major advantages of the common-drain amplifier over the common-source amplifier is that it offers smaller value of input capacitance as compared to the common-source amplifier.

The output admittance (Y_o) can also be determined in a manner similar to that for the common-drain JFET amplifier. It is given by

$$Y_o = g_m + g_d + j\omega C_T \tag{9.84}$$

9.7 High-Frequency Response of Cascaded Amplifier Stages

We have studied in Chapter 8 that the overall frequency response of an amplifier changes if an additional stage is added to it. In a multistage amplifier, the upper cut-off frequency is determined by the stage having the smallest value of the upper cut-off frequency.

The upper cut-off frequency (f_{Hn}) for "n" identical non-interactive stage amplifier is given by

$$f_{Hn} = f_H\sqrt{2^{1/n} - 1} \tag{9.85}$$

where f_H is the upper cut-off frequency of each individual stage. The upper cut-off frequency of a two-stage amplifier (f_{H2}) is therefore given by

$$f_{H2} = f_H\sqrt{2^{1/2} - 1} = 0.64 f_H \tag{9.86}$$

If in a multistage amplifier, the input impedance of the stages is low enough to act as a appreciable shunt on the output impedance of the stages preceding them, then it is no longer possible to isolate the stages. Under such conditions, individual 3 dB frequencies for different stages cannot be obtained in isolation. The 3 dB frequency in this case is obtained by considering the effect of each of the stages on the stages preceding and following them.

EXAMPLE 9.4 *For the cascaded amplifier shown in Figure 9.17, determine the overall upper cut-off frequency of the amplifier. Given that h_{ie} for each transistor is 1000 Ω, $r_{b'e}$ is 800 Ω, $r_{bb'}$ is 200 Ω, C_c is 5 pF, C_e is 40 pF and $g_m = 60 \times 10^{-3}$ mhos.*

Solution

1. The overall upper cut-off frequency can be determined by determining the upper cut-off frequency for each stage.

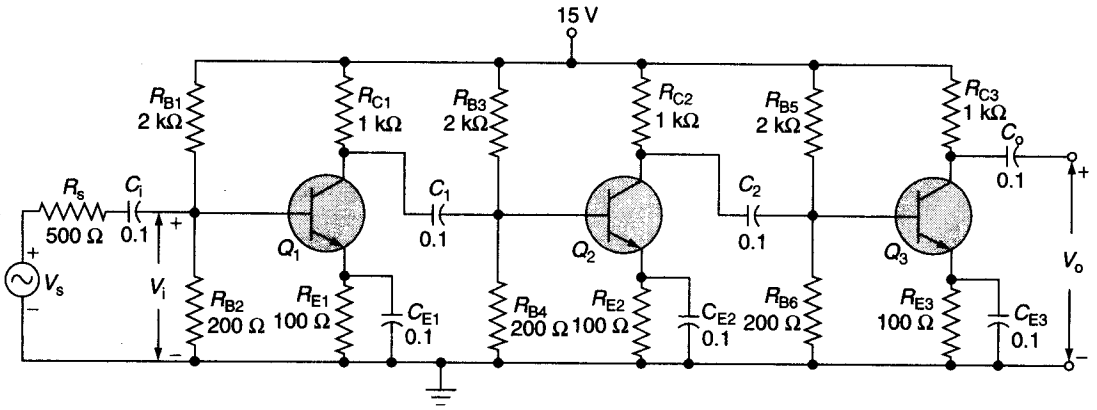


Figure 9.17 | Example 9.4.

2. The upper cut-off frequency for the third stage amplifier (f_{H3}) is given by

$$f_{H3} = \frac{1}{2\pi R_{3'}[C_e + C_c(1 + g_m R_{C3})]}$$

3.
$$R_{3'} = \frac{(R_{C2} \| R_{B5} \| R_{B6} + r_{bb'3}) \times r_{b'e3}}{(R_{C2} \| R_{B5} \| R_{B6} + h_{ie3})}$$
$$= \frac{(1000 \| 2000 \| 200 + 200) \times 800}{(1000 \| 2000 \| 200 + 1000)}$$
$$= \frac{(153.85 + 200) \times 800}{153.85 + 1000} = 245.34\ \Omega$$

4.
$$f_{H3} = \frac{1}{2 \times 3.1414 \times 245.34[40 \times 10^{-12} + 5 \times 10^{-12}(1 + 60 \times 10^{-3} \times 1 \times 10^{3})]}$$
$$= \frac{1}{2 \times 3.1414 \times 245.34 \times 345 \times 10^{-12}} = 1.88\ \text{MHz}$$

5. The upper cut-off frequency for the second stage (f_{H2}) is given by

$$f_{H2} = \frac{1}{2\pi R_{2'}[C_e + C_c(1 + g_m R_{L2'})]}$$

6. The effective value of load resistance for the second stage ($R_{L2'}$) is given by

$$R_{L2'} = R_{C2} \| R_{B5} \| R_{B6} \| h_{ie3}$$
$$= 1000 \| 2000 \| 200 \| 1000 = 133.33\ \Omega$$

7. The value of $R_{2'}$ is given by

$$R_{2'} = \frac{(R_{C1} \| R_{B3} \| R_{B4} + r_{bb'2}) \times r_{b'e2}}{(R_{C1} \| R_{B3} \| R_{B4} + h_{ie2})}$$
$$= \frac{(1000 \| 2000 \| 200 + 200) \times 800}{(1000 \| 2000 \| 200 + 1000)}$$
$$= \frac{(153.85 + 200) \times 800}{153.85 + 1000} = 245.34\,\Omega$$

8. $$f_{H2} = \frac{1}{2 \times 3.1414 \times 245.34[40 \times 10^{-12} + 5 \times 10^{-12}(1 + 60 \times 10^{-3} \times 133.33)]}$$
$$= 7.63 \text{ MHz}$$

9. The upper cut-off frequency for the first stage (f_{H1}) is given by

$$f_{H1} = \frac{1}{2\pi R_{1'}[C_e + C_c(1 + g_m R_{L1'})]}$$

10. The effective load resistance for the first stage ($R_{L1'}$) is given by

$$R_{L1'} = R_{C1} \| R_{B3} \| R_{B4} \| h_{ie2}$$
$$= 1000 \| 2000 \| 200 \| 1000$$
$$= 133.33\,\Omega$$

11. The value of $R_{1'}$ is given by

$$R_{1'} = \frac{(R_s \| R_{B1} \| R_{B2} + r_{bb'1}) \times r_{b'e1}}{(R_s \| R_{B1} \| R_{B2} + h_{ie1})}$$
$$= \frac{(500 \| 2000 \| 200 + 200) \times 800}{(500 \| 2000 \| 200 + 1000)}$$
$$= \frac{(133.33 + 200) \times 800}{133.33 + 1000} = 235.292\,\Omega$$

12. $$f_{H1} = \frac{1}{2 \times 3.1414 \times 235.292[40 \times 10^{-12} + 5 \times 10^{-12}(1 + 60 \times 10^{-3} \times 133.33)]}$$
$$= 7.96 \text{ MHz}$$

13. The overall upper cut-off frequency is limited by the cut-off frequency of the third stage as it is around four times less than the cut-off frequencies of the other two stages.

14. The overall upper cut-off frequency is therefore approximately equal to 1.88 MHz.

9.8 Amplifier Rise Time and Sag

The response of an amplifier to a step input is an effective measure to test its performance. There is a close relationship between the transfer function of the amplifier for the leading edge of the step input and its high-frequency response. In other words, the high-frequency response of the amplifier essentially determines the ability of the amplifier to faithfully respond to rapid variations in the input signal. Similarly, the response of the amplifier to the flat portion of the step input and its low-frequency response are interrelated. That is, the low-frequency response of the amplifier is a measure of the fidelity of the amplifier to respond to slowly varying changes in the input signal.

Rise Time

Let us consider that the step input applied has a pulse width of t_p. Figure 9.18 shows the response of the amplifier to the leading and the falling edge of the step input. The amplifier acts as a low pass filter to the leading and the falling edges of the input signal. The transfer function of the amplifier to the leading edge of the input signal is given by

$$V_o = V(1-e^{-t/R_1C_1}) \tag{9.87}$$

where R_1 and C_1 are the resistive and the capacitive elements limiting the high-frequency response of the amplifier. The rise-time (t_r) of the amplifier is given by the time required by the output signal to rise from 10% of its final value to 90% of its final value. It is an indication of how fast the amplifier responds to the fast rising edges of the input signal. The value of the rise time is given by

$$t_r = 2.2R_1C_1 = \frac{2.2}{2\pi f_H} = \frac{0.35}{f_H} \tag{9.88}$$

where f_H is the upper cut-off frequency of the amplifier. t_r is specified in s, ms and μs respectively, for f_H in Hz, kHz and MHz. Therefore, the rise time of an amplifier is inversely proportional to its upper 3 dB cut-off frequency. The upper 3 dB frequency of the amplifier (f_H) required to amplify the step input signal with pulse width t_p, without much distortion is given by

$$f_H = \frac{1}{t_p} \tag{9.89}$$

Substituting the value of f_H in Eq. (9.88), we get

$$t_r = 0.35t_p \tag{9.90}$$

Tilt or Sag

The response of the amplifier to the flat portion of the step input (Figure 9.19) is affected by the high-pass circuit of the amplifier. The transfer function is expressed as

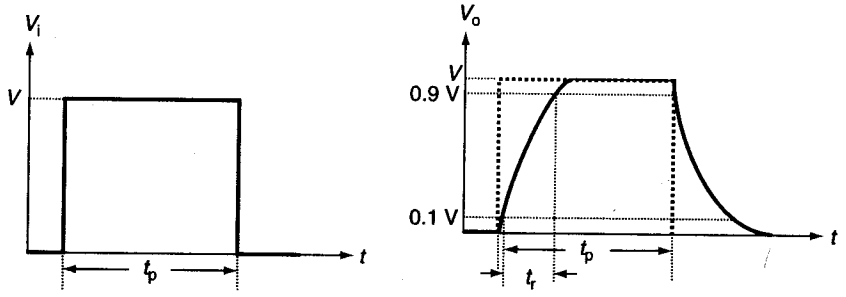


Figure 9.18 | Response of the amplifier to the leading and the falling edges of the step input.

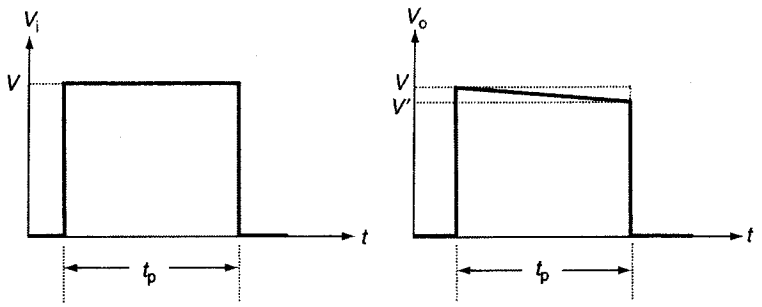


Figure 9.19 | Response of the amplifier to the flat portion of the step input.

$$V_o = Ve^{-t/R_2C_2} \tag{9.91}$$

where R_2 and C_2 are the resistive and the capacitive elements limiting the low-frequency response of the amplifier. For time t, much larger than the time constant R_2C_2, Eq. (9.91) can be approximated as

$$V_o = V\left(1 - \frac{t}{R_2C_2}\right) \tag{9.92}$$

From Figure 9.19, the percentage tilt or sag in the output voltage is given by

$$P = \left(\frac{V - V'}{V}\right) \times 100\% = \left(\frac{t_p}{R_2C_2}\right) \times 100\% \tag{9.93}$$

where t_p is the pulse width of the step input.

KEY TERMS

Hybrid-Π model
Giacoletto model
β cut-off frequency (f_β)
Short-circuit gain-bandwidth product (f_T)
α cut-off frequency (f_α)
Miller's theorem
Rise-time
Sag

OBJECTIVE-TYPE EXERCISES

Multiple-Choice Questions

1. The emitter diffusion capacitance for a transistor
   a. is directly proportional to the collector current.
   b. is inversely proportional to the collector current.
   c. is independent of the collector current.
   d. is proportional to the square of collector current.

2. The rise time of an amplifier is
   a. inversely proportional to the upper 3 dB cut-off frequency.
   b. directly proportional to the upper 3 dB cut-off frequency.
   c. independent of the upper 3 dB cut-off frequency.
   d. proportional to the square root of the upper 3 dB cut-off frequency.

3. The value of α cut-off frequency is
   a. smaller than the β cut-off frequency.
   b. greater than the β cut-off frequency.
   c. can be more or less than the β cut-off frequency.

d. equal to the β cut-off frequency.

4. The conductance ($g_{b'c}$) takes into account
   a. the resistance between the emitter and the collector terminals.
   b. the conductance between the base and collector due to flow of majority carriers.
   c. the reduction in the flow of emitter current.
   d. the feedback effect between the output and the input due to the Early effect.
5. The Ohmic base-spreading resistance is represented as
   a. the increase in the recombination base currrent due to the increase in the minority carriers in the base region.
   b. the conductance between the collector and the emitter terminals.
   c. a lump parameter between the external base terminal and the node B′.
   d. the feedback effect between the output and the input due to the Early effect.

State whether True or False

1. The response of the amplifier to the flat portion of the step input is affected by the high-pass circuit of the amplifier.
2. The value of the gain-bandwidth product of the common-emitter amplifier increases with increase in the value of the collector current.
3. The value of the transistor's transconductance decreases with increase in temperature
4. α cut-off frequency is the frequency at which the short-circuit small signal forward current transfer ratio of a common-base amplifier drops by 3 dB to its value at low frequencies.
5. The common-base transistor amplifier has a higher value of upper cut-off frequency than the common-emitter transistor amplifier.

REVIEW QUESTIONS

1. Draw the hybrid-Π model of a transistor, explaining each of the components used in the model.
2. What do you understand by the term "rise-time"? Which parameters affect the rise time in case of a bipolar transistor-based amplifier?
3. When different identical amplifier stages are connected in cascade, which stage has the most influence on the overall high-frequency response of the amplifier and why?
4. What is Miller's effect? What influence does it have on the high-frequency response of the transistor or FET amplifier?
5. Derive the expressions for the upper cut-off frequencies of the common-emitter and the common-base transistor amplifier configurations?
6. Explain why the 3 dB frequency for the current gain is not the same as the 3 dB frequency for the voltage gain.
7. Derive the expression for the short-circuit current gain of a common-emitter transistor amplifier as a function of frequency.
8. Using Miller's theorem, derive the expression for the mid-band input capacitance of a common-emitter transistor amplifier with load resistance.
9. Draw the small signal equivalent circuit for a common-source MOSFET amplifier.
10. Differentiate between:
    a. The α cut-off frequency and the β cut-off frequency.
    b. The high-frequency response of a common-collector amplifier and a common-emitter amplifier.
    c. Hybrid parameters for low-frequency analysis and hybrid-Π parameters for high-frequency analysis.

PROBLEMS

1. Calculate the voltage gain at operating frequencies of 20 kHz and 20 MHz of the common-drain MOSFET amplifier with source resistance (R_S) of 1 kΩ. The MOSFET parameters are g_m = 1.5 mA/V, r_d = 50 kΩ, C_{gs} = 2.5 pF, C_{ds} = 1.0 pF, C_{gd} = 2.8 pF and C_{sn} = 2.7 pF.

2. For the cascaded amplifier shown in Figure 9.20, determine the overall upper cut-off frequency of the amplifier. Given that h_{fe} of each transistor is 100, h_{ie} is 850 Ω, $r_{b'e}$ is 600 Ω, $r_{bb'}$ is 250 Ω, C_c is 10 pF, C_e is 50 pF and $g_m = 1.50 \times 10^{-3}$ mhos.

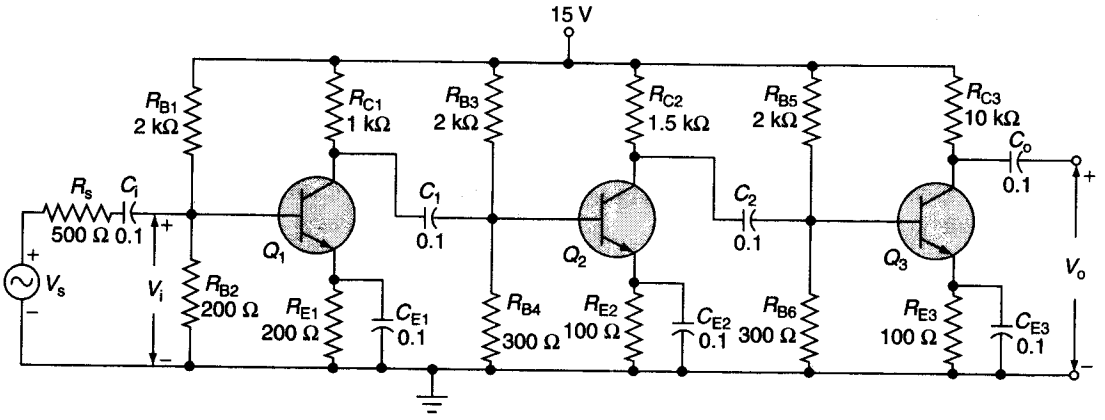


Figure 9.20 | Problem 2.

3. The bandwidth of a single-stage amplifier extends from 10 Hz to 100 kHz. Find the frequencies at which the voltage gain is down by 1 dB from its mid-band value.

4. A three-stage amplifier with identical stages has an overall lower and upper 3 dB cut-off frequencies of 10 Hz and 10 kHz, respectively. Determine the upper and the lower cut-off frequencies of the individual stages assuming that the stages are non-interactive stages.

ANSWERS

Multiple-Choice Questions

1. (a) 2. (a) 3. (b) 4. (d) 5. (c)

State whether True or False

1. True
2. False
3. True
4. True
5. True

Problems

1. 0.595, 0°, 0.581, −5.37°
2. 2.868 MHz
3. 19.65 Hz, 51 kHz
4. 19.61 kHz, 5.1 Hz